

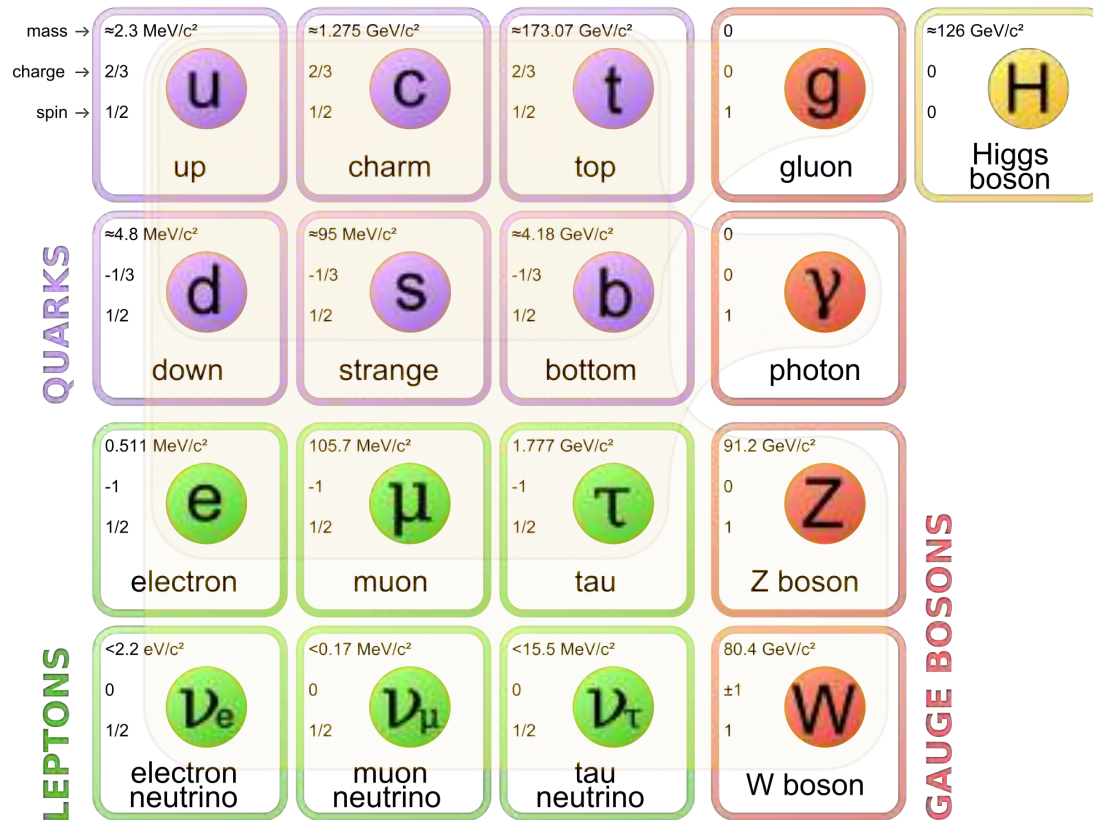
# A new era of pixel detectors for future High Energy Physics experiments

**Sonia Fernandez-Perez**

Workshop física teorica UVA– 27.05.2016

- The Large Hadron Collider (LHC)
- The ATLAS detector
- The HL- LHC program
- Basic working principle and challenges of pixel detectors
- Pixel detectors developments for ATLAS at HL-LHC

- The Standard Model describes all elementary particles and their interactions
- It is incomplete (no explanation to gravitational interactions, dark matter, asymmetry matter-antimatter, etc)



# The Large Hadron Collider

- The Standard Model describes all elementary particles and their interactions
- It is incomplete (no explanation to gravitational interactions, dark matter, asymmetry matter-antimatter, etc)



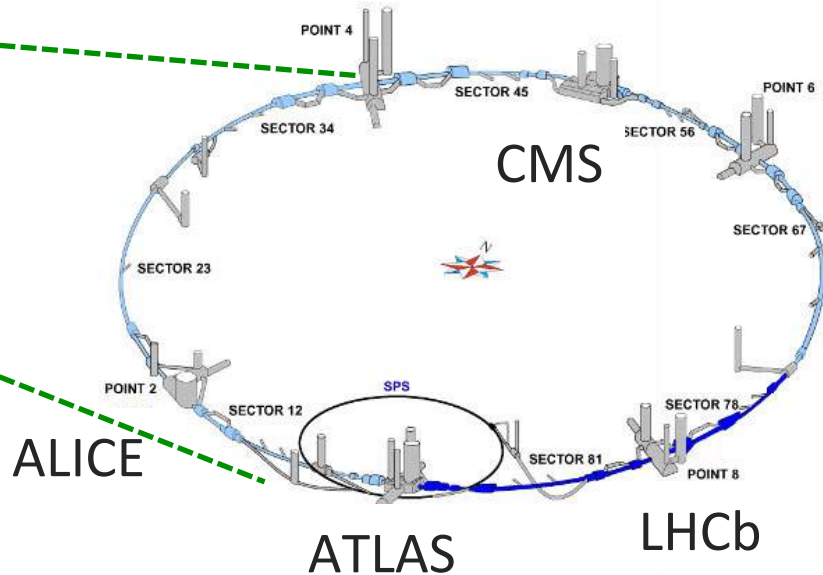
- proton-proton collider
- 27 km circumference
- 100 m underground
- During the first data taking period Run 1 (2009-2012) luminosity of  $10^{34} \text{ cm}^{-2}\text{s}^{-1}$ , collision energy of 7-8 TeV, and 50 ns bunch crossing.
- 4 main experiments: ALICE, ATLAS, CMS, LHCb

# The Large Hadron Collider

- The Standard Model describes all elementary particles and their interactions
- It is incomplete (no explanation to gravitational interactions, dark matter, asymmetry matter-antimatter, etc)



- proton-proton collider
- 27 km circumference
- 100 m underground
- 4 main experiments: ALICE, ATLAS, CMS, LHCb



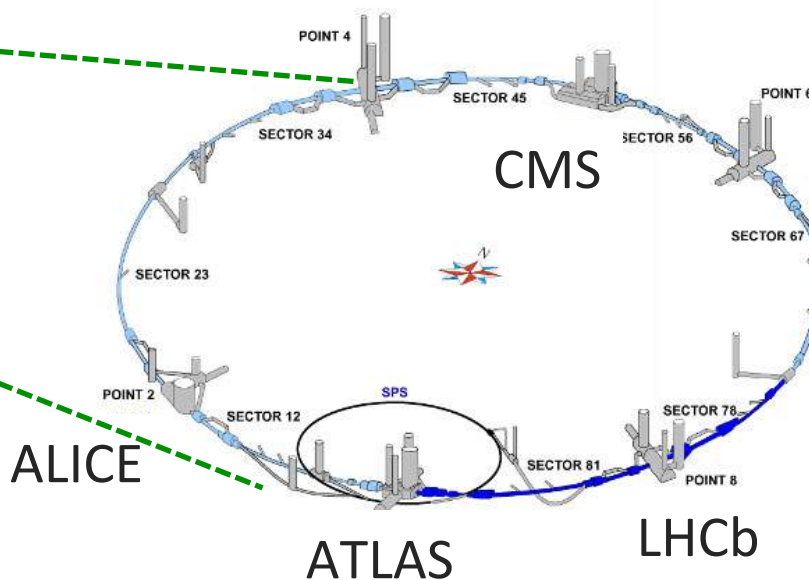
# The Large Hadron Collider

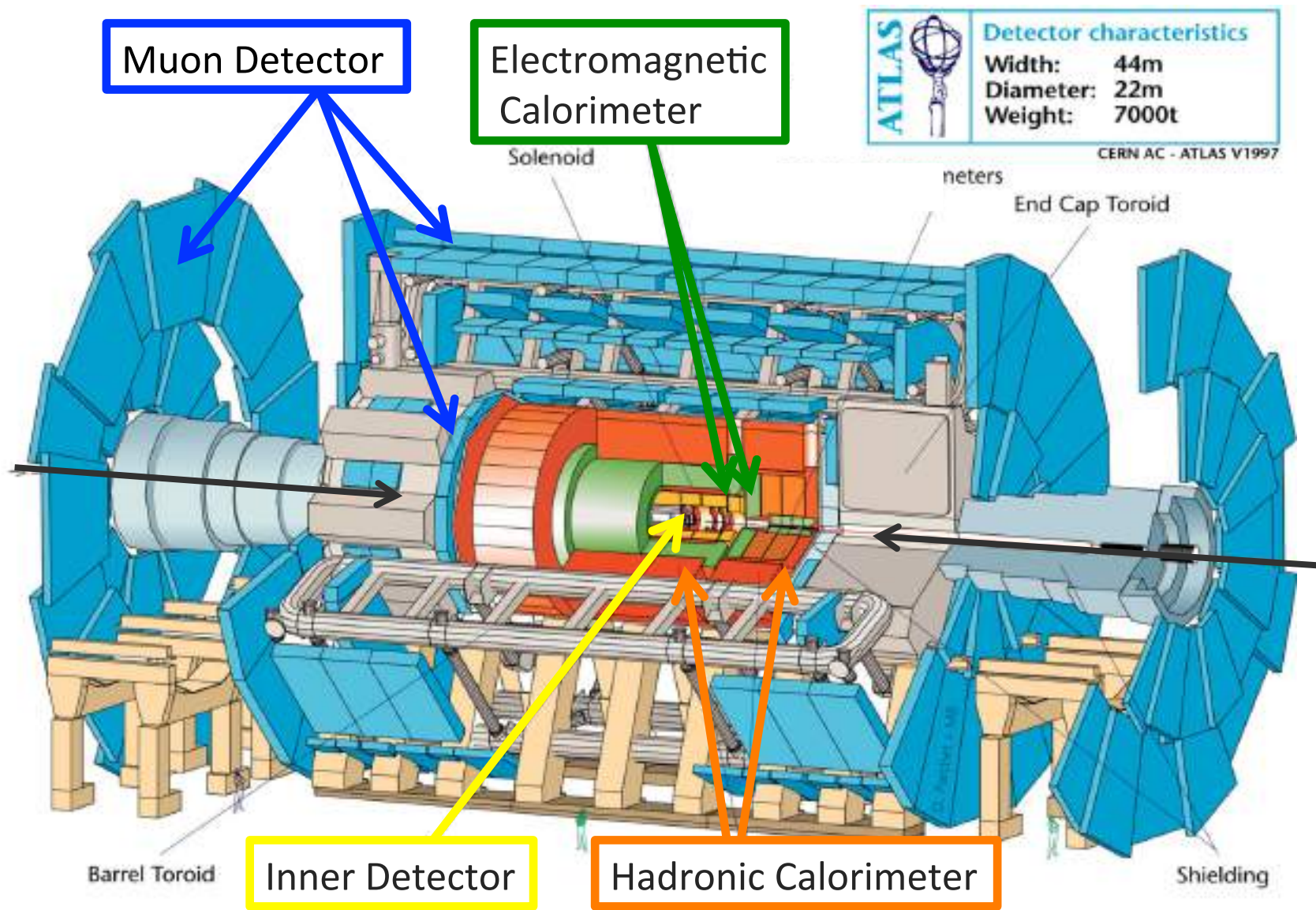
- The Standard Model describes all elementary particles and their interactions
- It is incomplete (no explanation to gravitational interactions, dark matter, asymmetry matter-antimatter, etc)

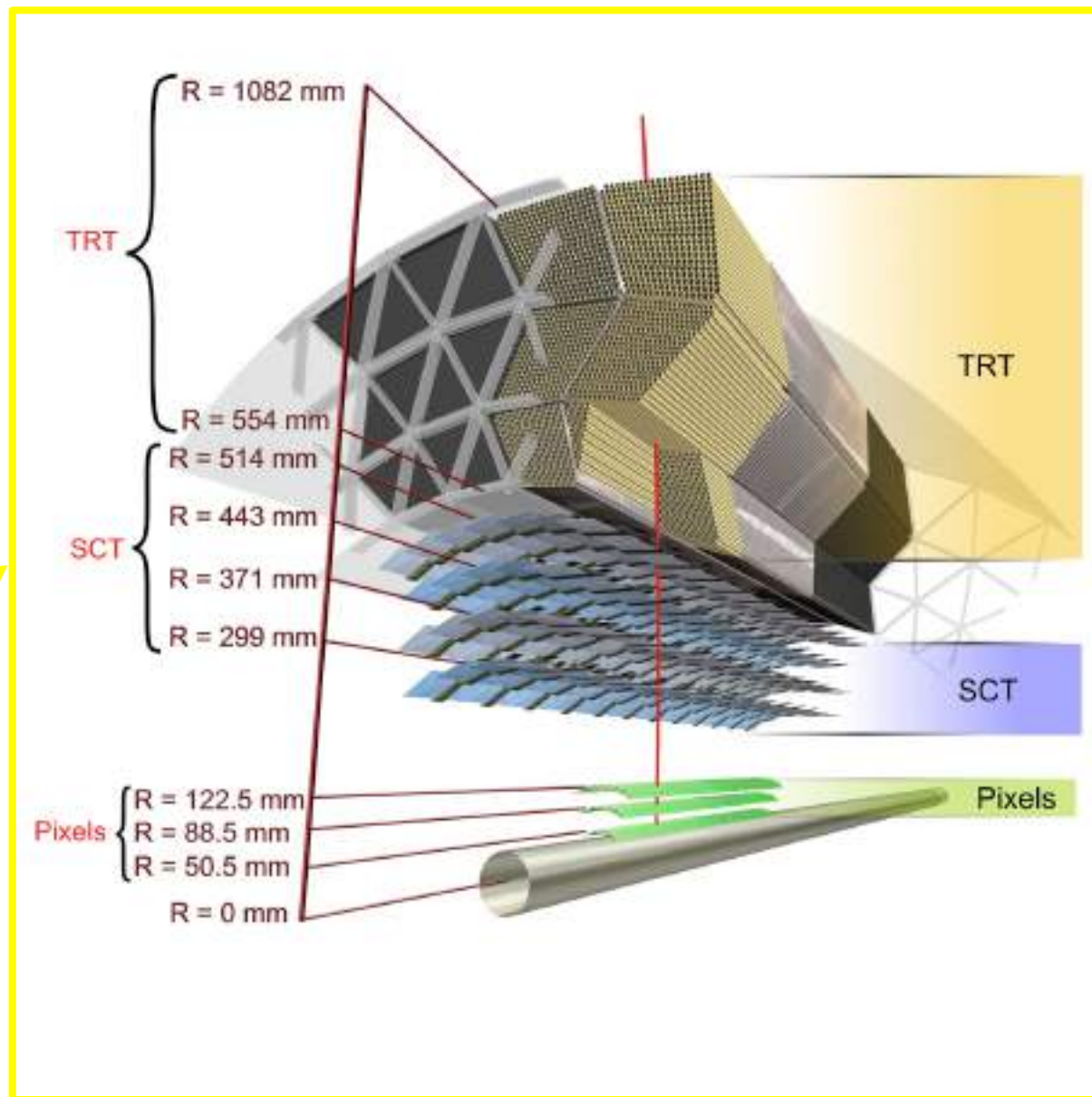


- proton-proton collider
- 27 km circumference
- 100 m underground
- 4 main experiments: ALICE, ATLAS, CMS, LHCb

Higgs discovery (2012)

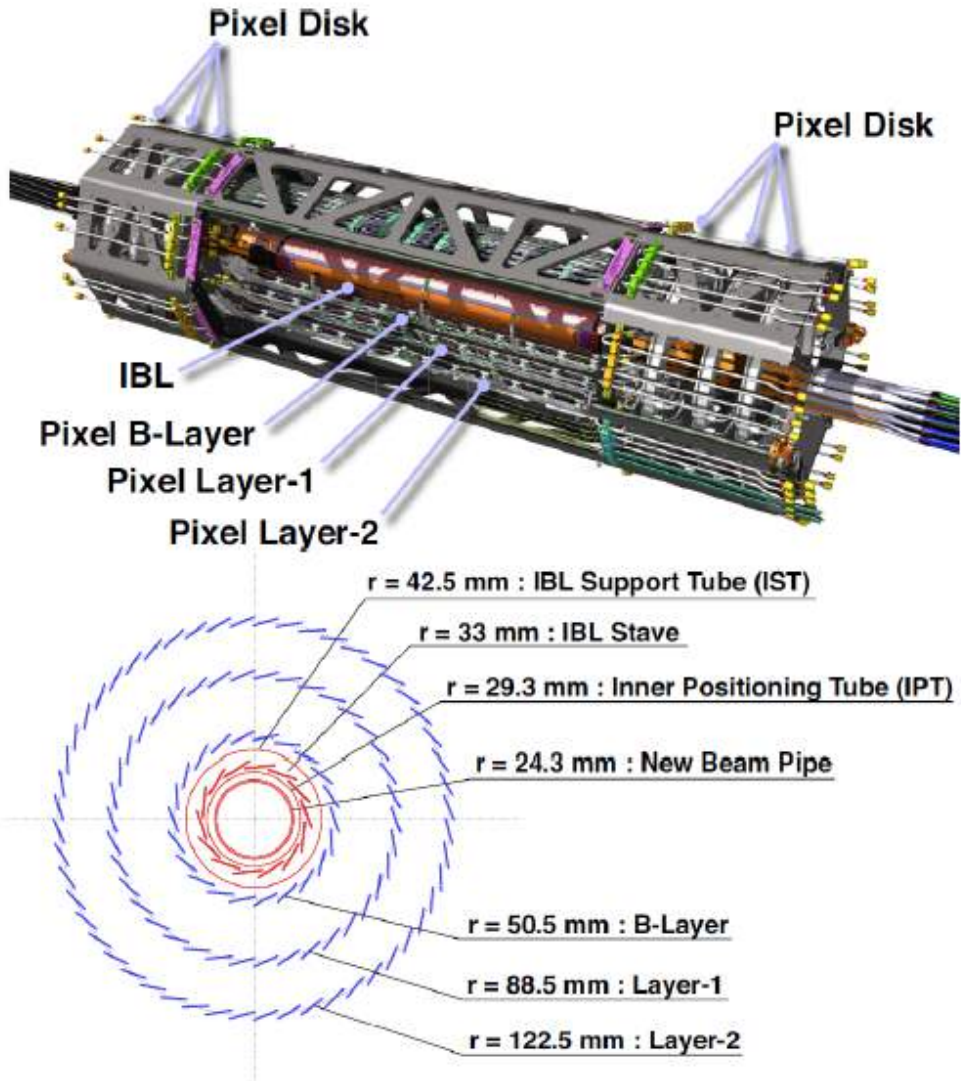






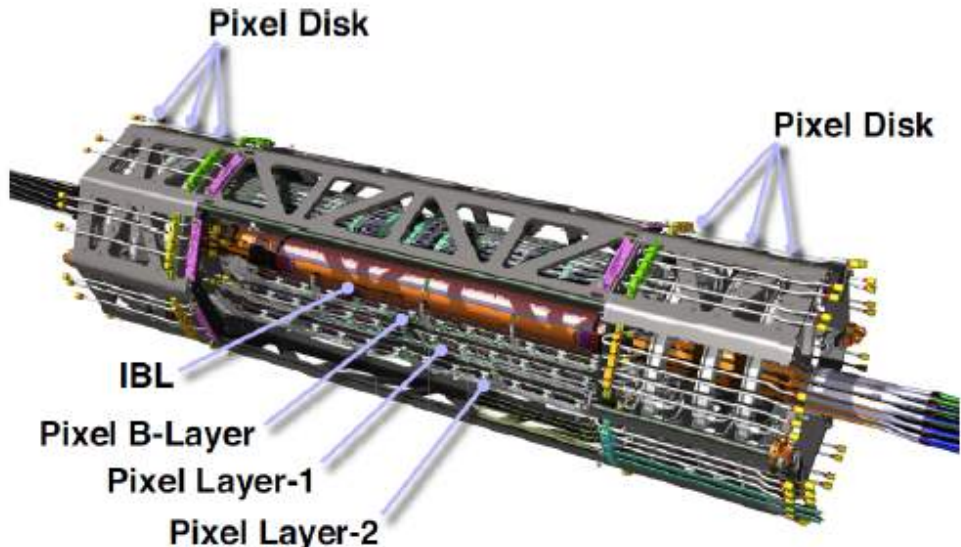
Inner Detector





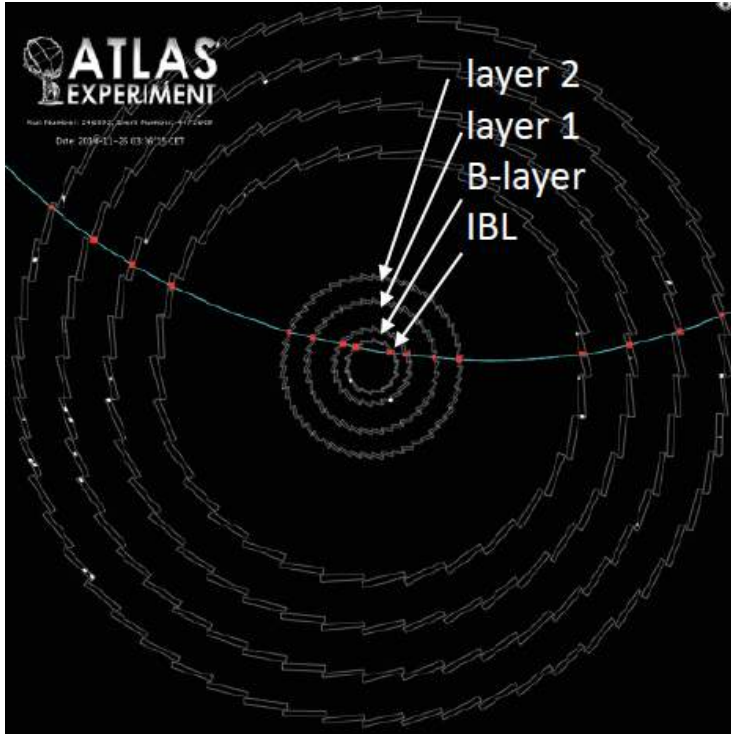
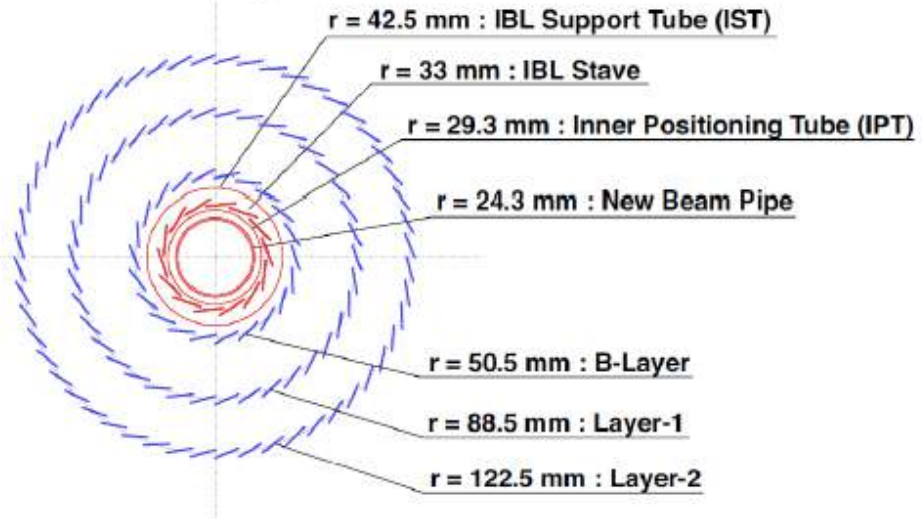
- The Pixel Detector is exposed to the harshest conditions
- 4 silicon detector layers

**Insertable B-Layer (IBL) installed in 2014**

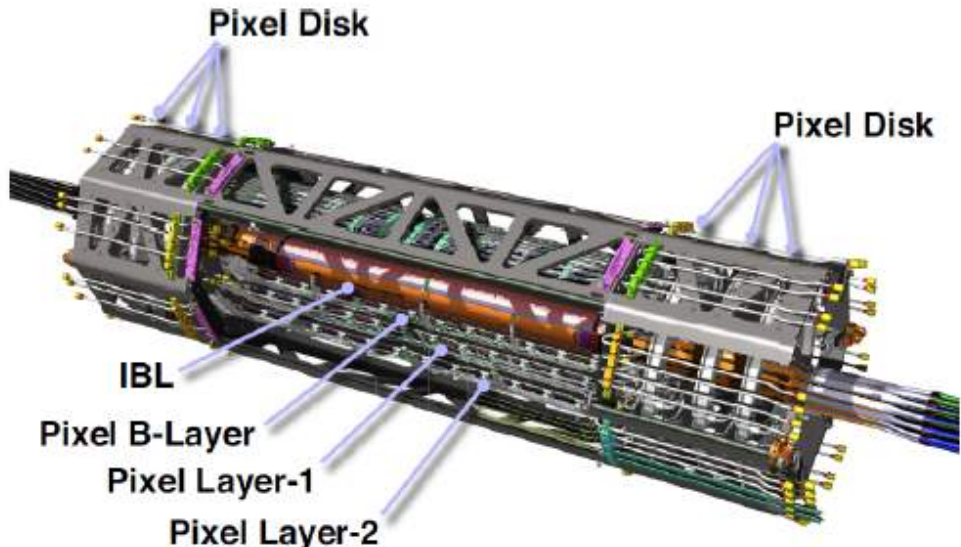


- The Pixel Detector is exposed to the harshest conditions
- 4 silicon detector layers

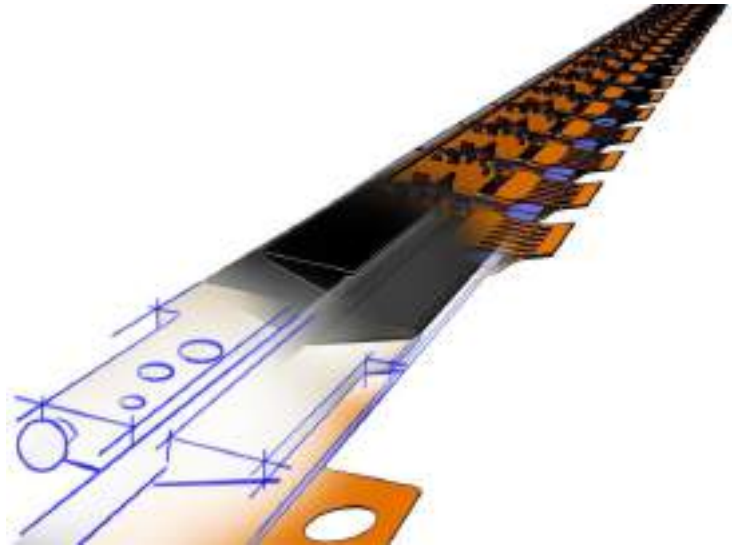
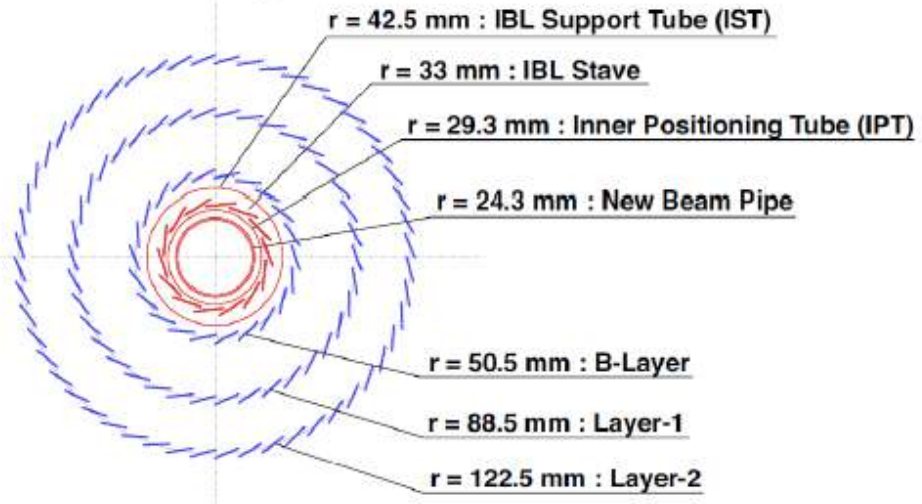
A true 4-hit pixel system!



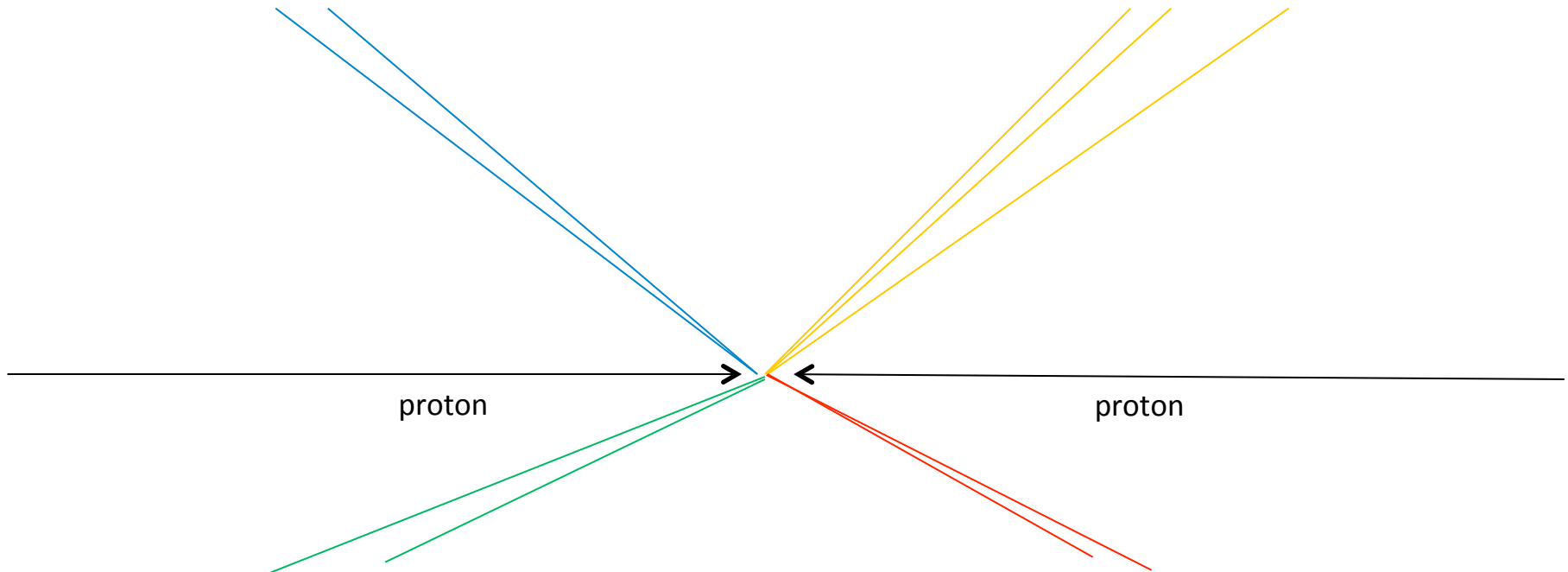
**Insertable B-Layer (IBL) installed in 2014**



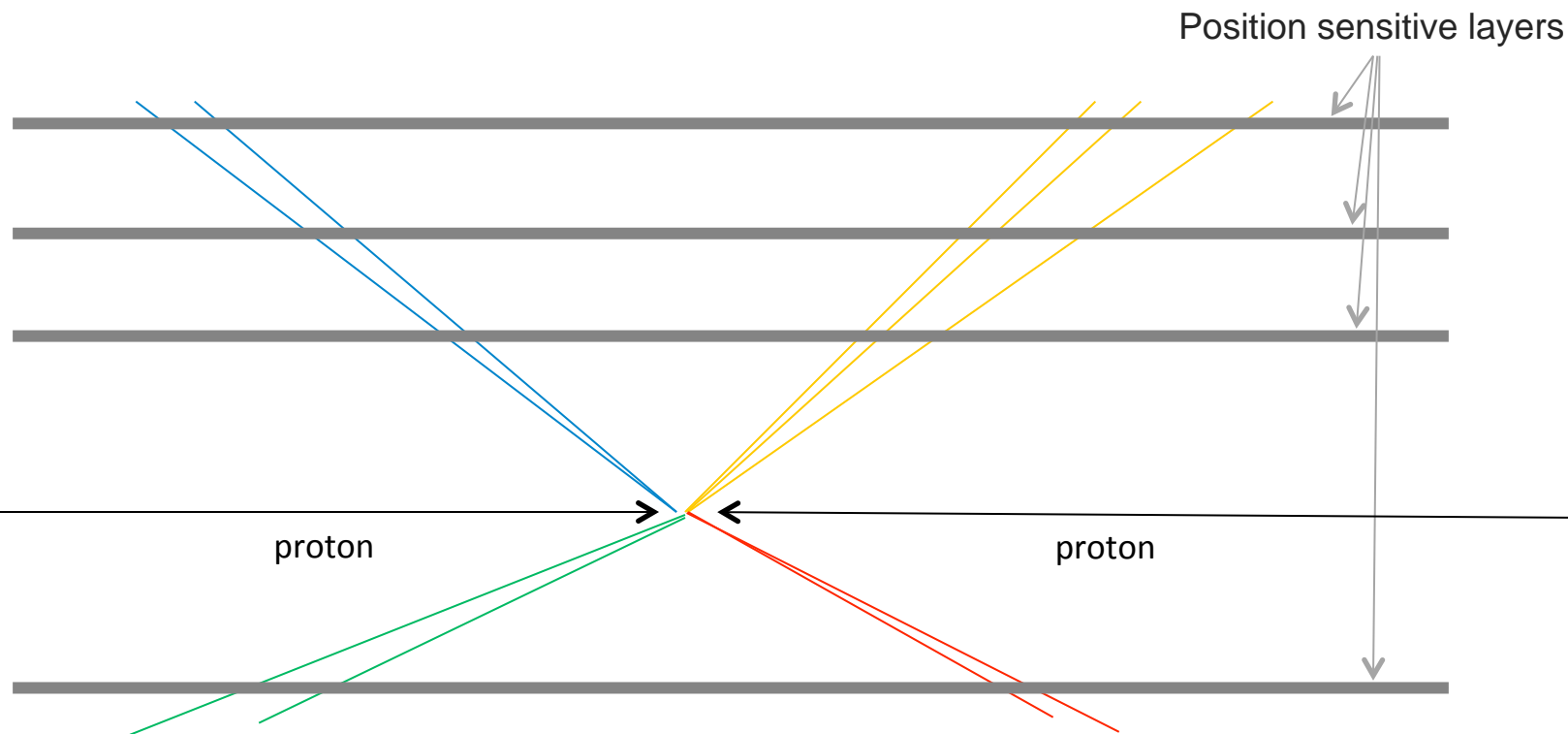
- The Pixel Detector is exposed to the harshest conditions
- 4 silicon detector layers
- Each layer is composed of 2D segmented silicon detectors



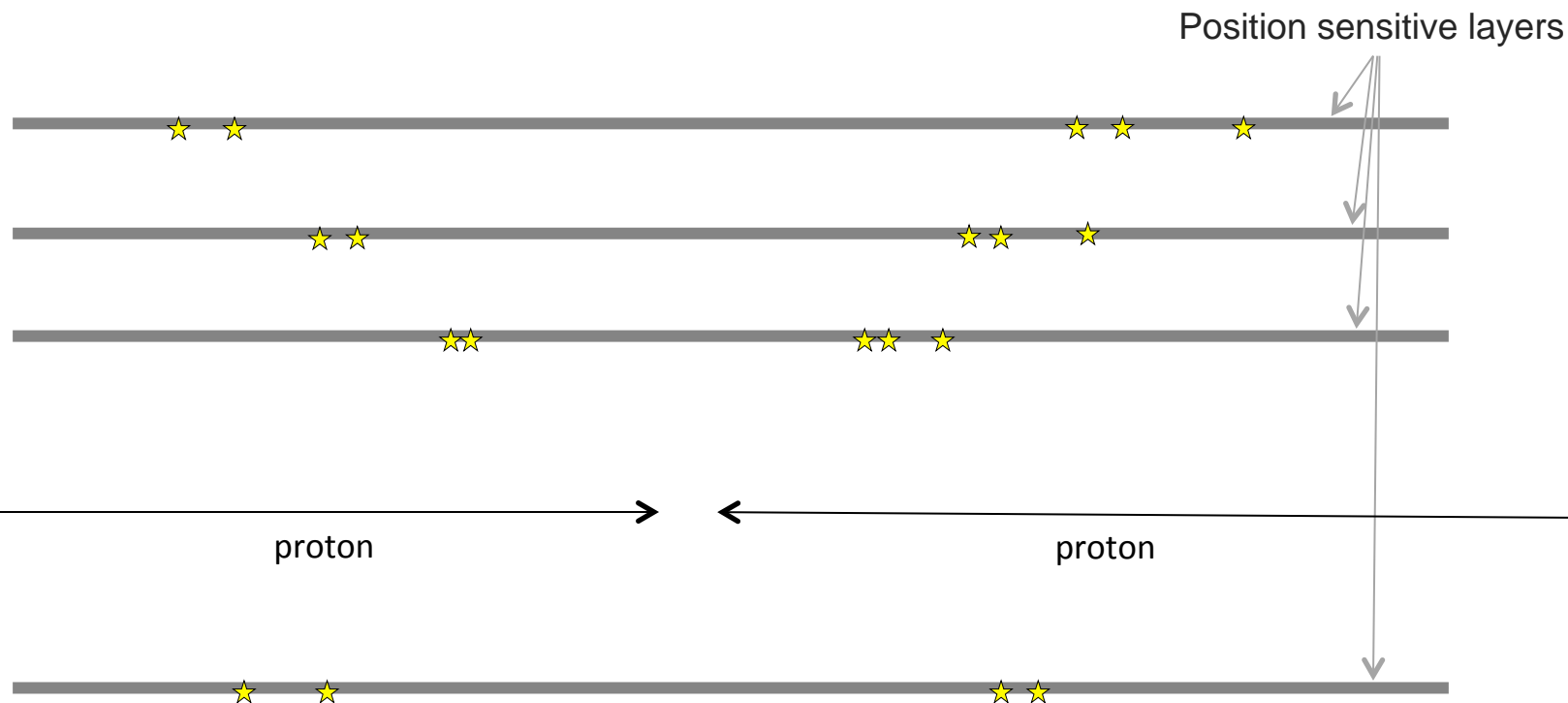
- Layers of segmented silicon detectors
- The energy loss by the particle while traversing the detector → electrical signal



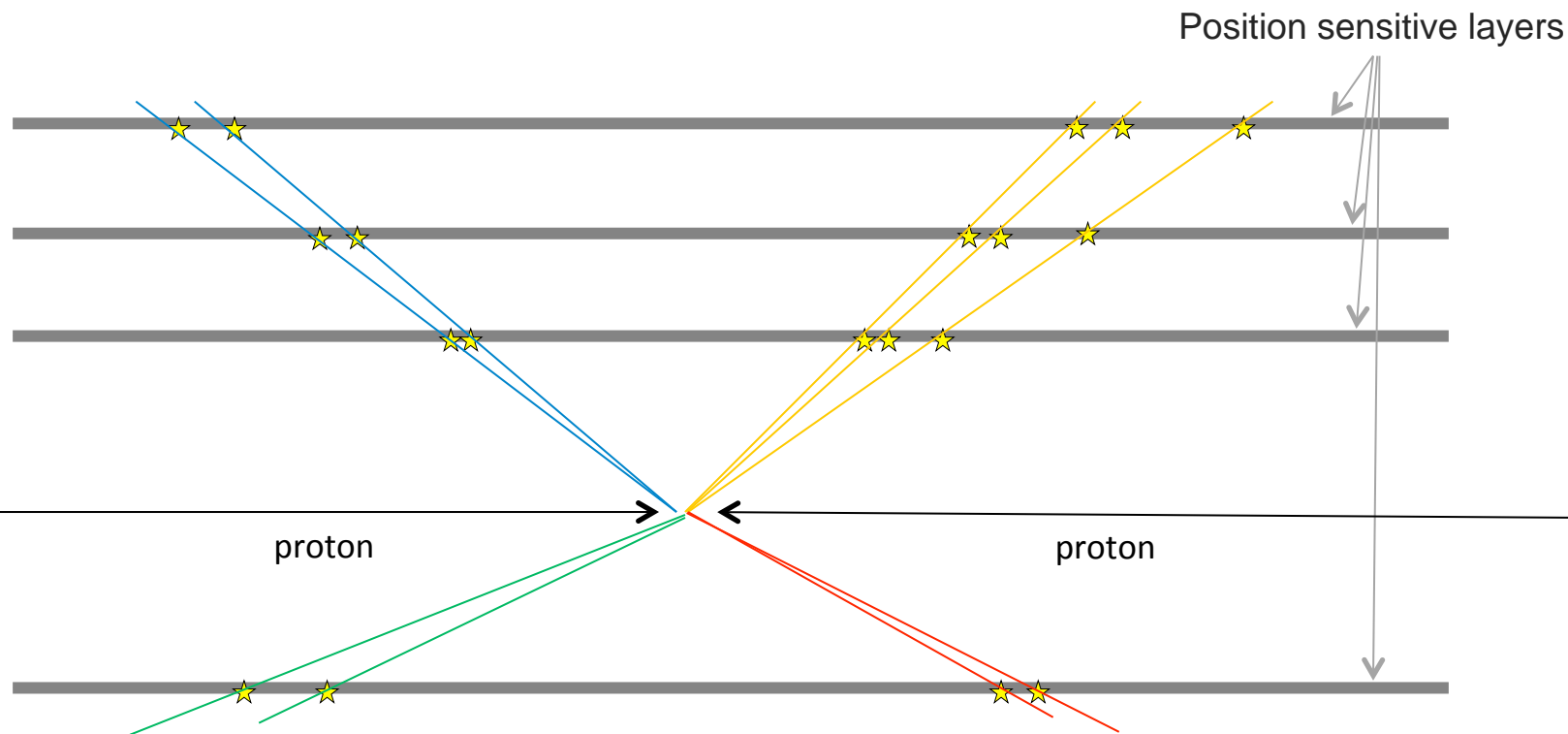
- Layers of segmented silicon detectors
- The energy loss by the particle while traversing the detector → electrical signal



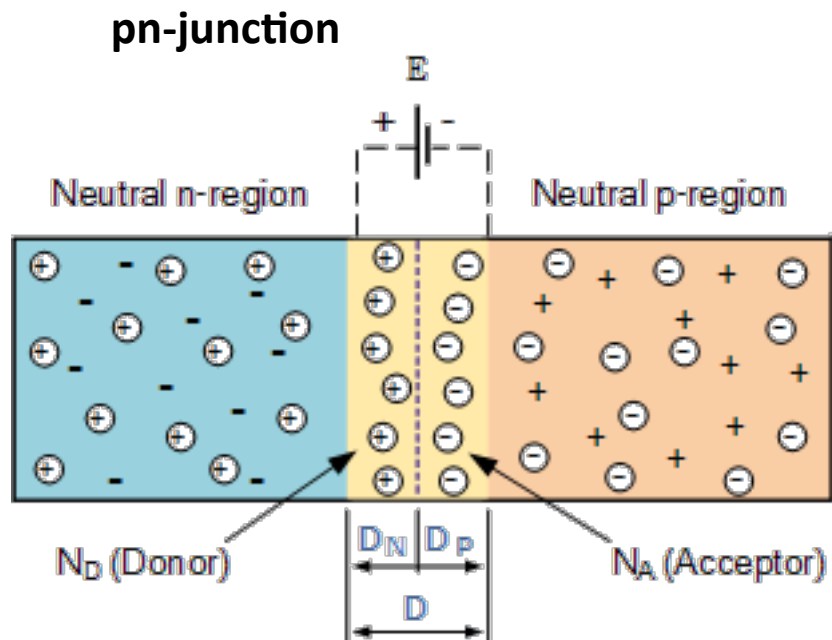
- Layers of segmented silicon detectors
- The energy loss by the particle while traversing the detector → electrical signal



- Layers of segmented silicon detectors
- The energy loss by the particle while traversing the detector → electrical signal



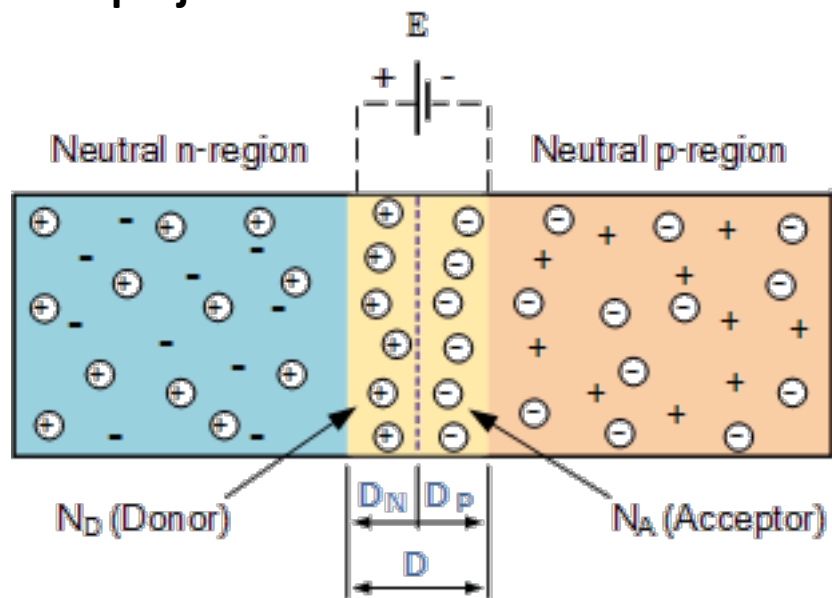
- pixel sensor: a 2D segmented pn-diode (reverse bias  $\rightarrow$  depletion zone)



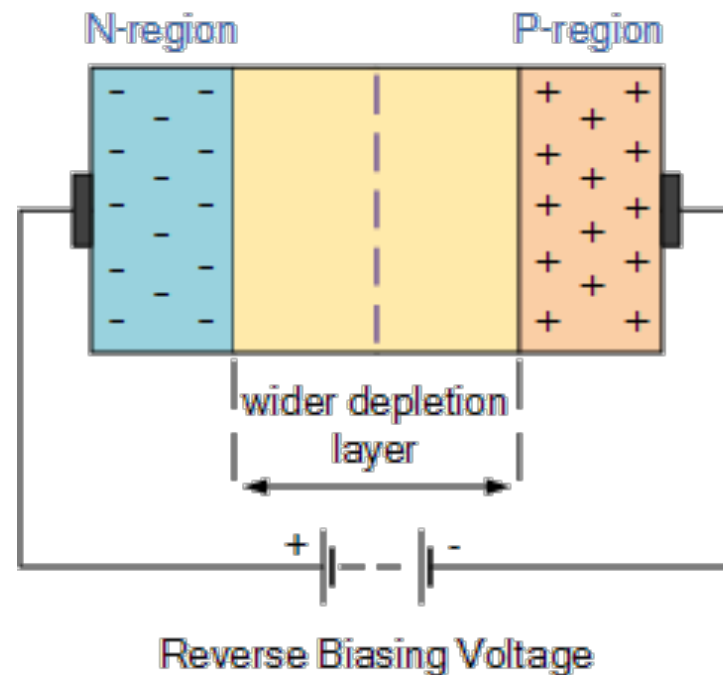


- pixel sensor: a 2D segmented pn-diode (reverse bias  $\rightarrow$  depletion zone)

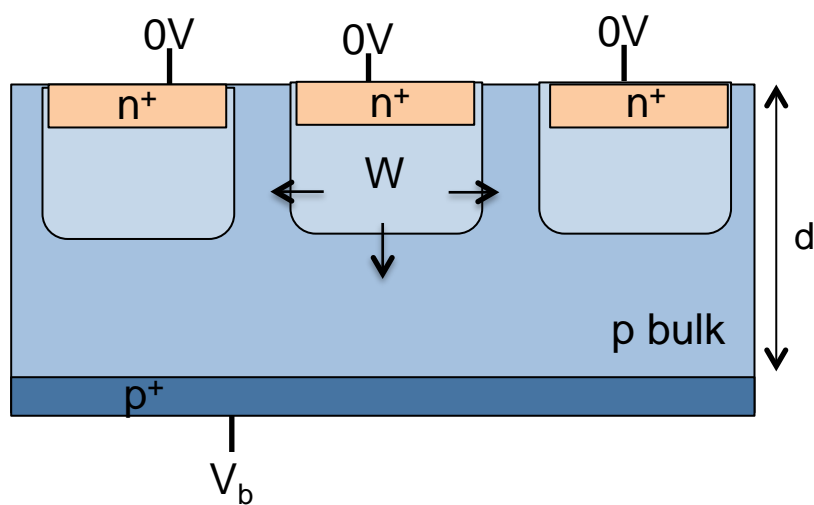
### pn-junction



### Reverse bias pn-junction

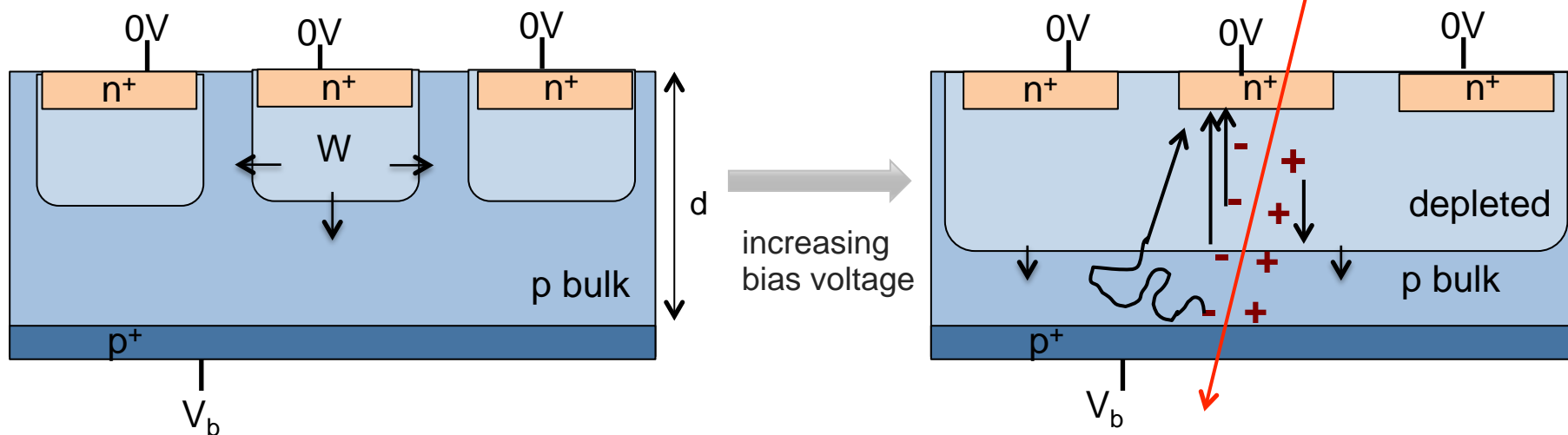


- pixel sensor: a 2D segmented pn-diode (reversely bias  $\rightarrow$  depletion zone)
- Depletion zone is the zone without free charge carriers



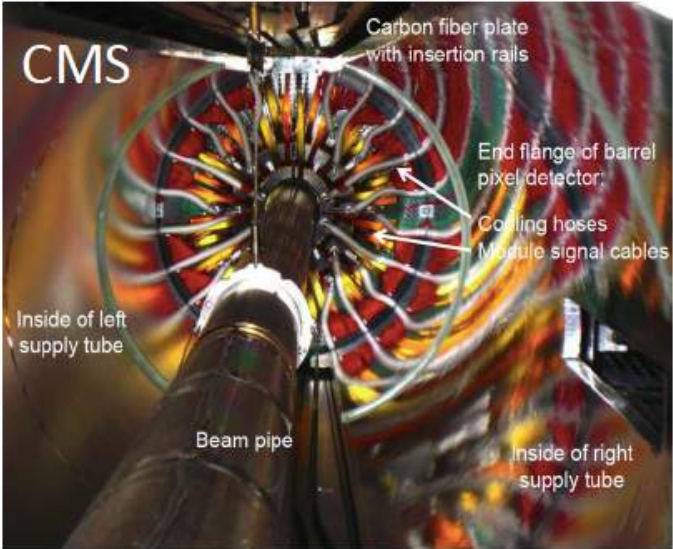
$$W = \sqrt{2 \epsilon \mu \rho V_b}$$

- pixel sensor: a 2D segmented pn-diode (reversely bias  $\rightarrow$  depletion zone)
- Depletion zone is the zone without free charge carriers

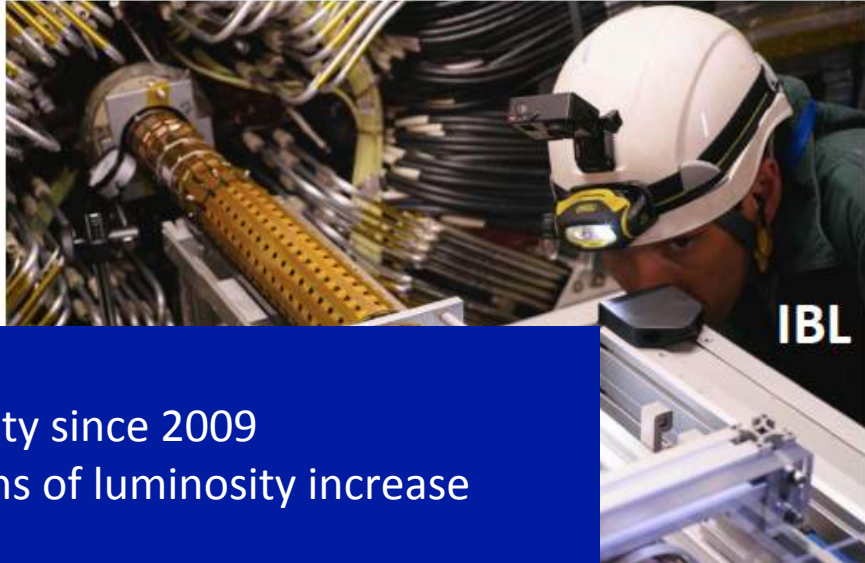
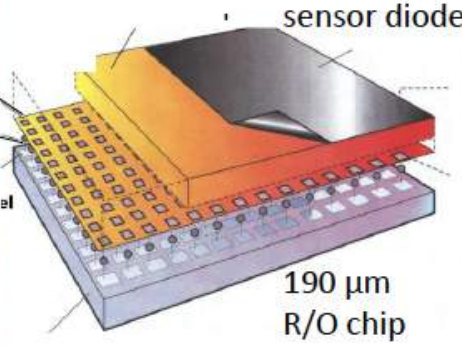


$$W = \sqrt{2 \epsilon \mu \rho V_b}$$

- A particle traversing the sensor generates electron-hole pairs
- Signal generation  $\rightarrow$  drift and diffusion
- ATLAS requirements: drift
- The signal is amplified and digitized in a R/O chip



all based on  
"Hybrid Pixels"



- Very good performance and reliability since 2009
- Not sufficient for long term LHC plans of luminosity increase

- Why do we need high luminosity?

frequency to obtain an specific event:

$$N_{\text{event}} = \text{Luminosity} \times \sigma_{\text{event}}$$

$$\sigma (pp) = 10^{11} \text{ pb}$$

$$\sigma (W/Z) = 10^4 \text{ pb}$$

$$\sigma (H) = 100 \text{ pb}$$



- Why do we need high luminosity?

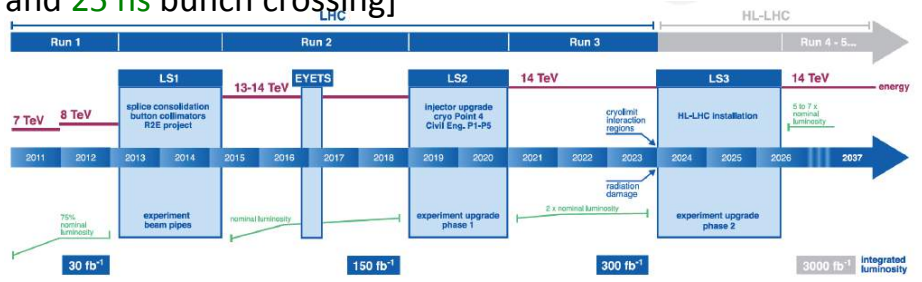
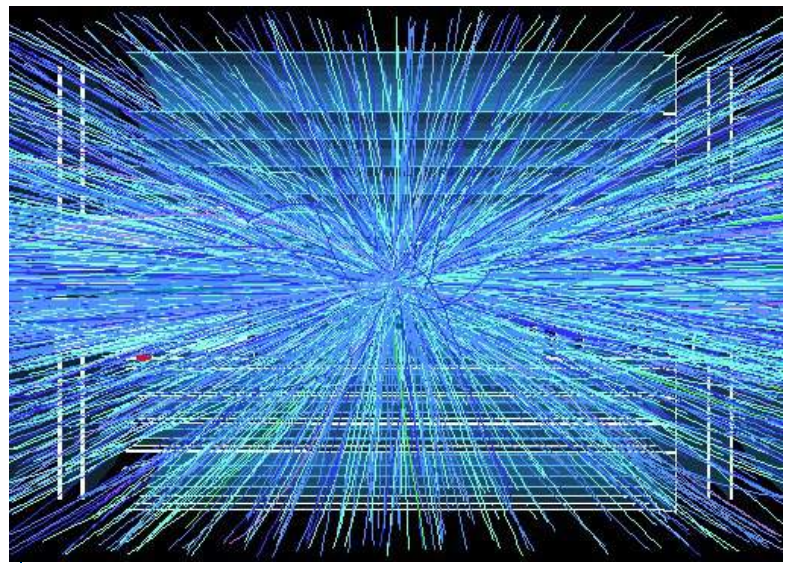
frequency to obtain an specific event:

$$N_{\text{event}} = \text{Luminosity} \times \sigma_{\text{event}}$$

- $\sigma(\text{pp}) = 10^{11} \text{ pb}$
- $\sigma(\text{W/Z}) = 10^4 \text{ pb}$
- $\sigma(\text{H}) = 100 \text{ pb}$



- The LHC plans to increase by a factor of 7 the luminosity in 2026 → **HL-LHC program** [luminosity of  $7 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ , collision energy of 14 TeV, and 25 ns bunch crossing]



Detector implications:

- Radiation hard detectors
- High rate
- Fast detectors

- The full Inner Detector of ATLAS will be replaced by a new all-silicon detector
  - Pixels and Strips
- The Pixel Detector layout is under discussion (4-6 layers)
- The requirements are at least one order of magnitude higher

# Introduction The ATLAS Inner Tracker (ITk)

- The full Inner Detector of ATLAS will be replaced by a new all-silicon detector
  - Pixels and Strips
- The Pixel Detector layout is under discussion (4-6 layers)
- The requirements are at least one order of magnitude higher

	Pixels LHC	IBL	Pixels HL-LHC (inner layers)	Pixels HL-LHC (outer layers)
Particle rate	1 MHz/mm <sup>2</sup>	5 MHz/mm <sup>2</sup>	10 MHz/mm <sup>2</sup>	1 MHz/mm <sup>2</sup>
Total Ionizing Dose (TID)	50 Mrad	250 Mrad	1 Grad	50 Mrad
Non Ionizing Energy Loss (NIEL)	10 <sup>15</sup> n <sub>eq</sub> cm <sup>-2</sup>	5 × 10 <sup>15</sup> n <sub>eq</sub> cm <sup>-2</sup>	2 × 10 <sup>16</sup> n <sub>eq</sub> cm <sup>-2</sup>	1 × 10 <sup>15</sup> n <sub>eq</sub> cm <sup>-2</sup>
Silicon Area	≈1.73 m <sup>2</sup>	≈0.15 m <sup>2</sup>	≈1 m <sup>2</sup>	≈10 - 20 m <sup>2</sup>
Pile-up	23	23	200	-



# Introduction The ATLAS Inner Tracker (ITk)

- The full Inner Detector of ATLAS will be replaced by a new all-silicon detector
  - Pixels and Strips
- The Pixel Detector layout is under discussion (4-6 layers)
- The requirements are at least one order of magnitude higher

	Pixels LHC	IBL	Pixels HL-LHC (inner layers)	Pixels HL-LHC (outer layers)
Particle rate	1 MHz/mm <sup>2</sup>	5 MHz/mm <sup>2</sup>	10 MHz/mm <sup>2</sup>	1 MHz/mm <sup>2</sup>
Total Ionizing Dose (TID)	50 Mrad	250 Mrad	1 Grad	50 Mrad
Non Ionizing Energy Loss (NIEL)	10 <sup>15</sup> n <sub>eq</sub> cm <sup>-2</sup>	5 × 10 <sup>15</sup> n <sub>eq</sub> cm <sup>-2</sup>	2 × 10 <sup>16</sup> n <sub>eq</sub> cm <sup>-2</sup>	1 × 10 <sup>15</sup> n <sub>eq</sub> cm <sup>-2</sup>
Silicon Area	≈1.73 m <sup>2</sup>	≈0.15 m <sup>2</sup>	≈1 m <sup>2</sup>	≈10 - 20 m <sup>2</sup>
Pile-up	23	23	200	-

Hybrid technology

Planar Pixel Sensor (PPS)

Hybrid technology

Planar Pixel Sensor (PPS)

3D Silicon sensor (3D)





- The full Inner Detector of ATLAS will be replaced by a new all-silicon detector
  - Pixels and Strips
- The Pixel Detector layout is under discussion (4-6 layers)
- The requirements are at least one order of magnitude higher

	Pixels LHC	IBL	Pixels HL-LHC (outer layers)
Particle rate	1 MHz/mm <sup>2</sup>		1 MHz/mm <sup>2</sup>
Total Ionizing Dose (TID)	50 Mrad		50 Mrad
Non Ionizing Energy Loss (NIEL)			$1 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$
Silicon Area		$\approx 1 \text{ m}^2$	$\approx 10 - 20 \text{ m}^2$
Pile-up		200	-

**International R&D effort for the new pixel detectors generation**

Hybrid technology  
 Sensor (PPS) Planar Pixel Sensor (PPS)  
 3D Silicon sensor (3D)

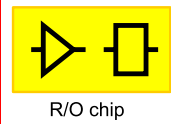
Inner layers

1. Radiation hardness
2. Low power consumption
3. Low material
4. Occupancy

Outer layers

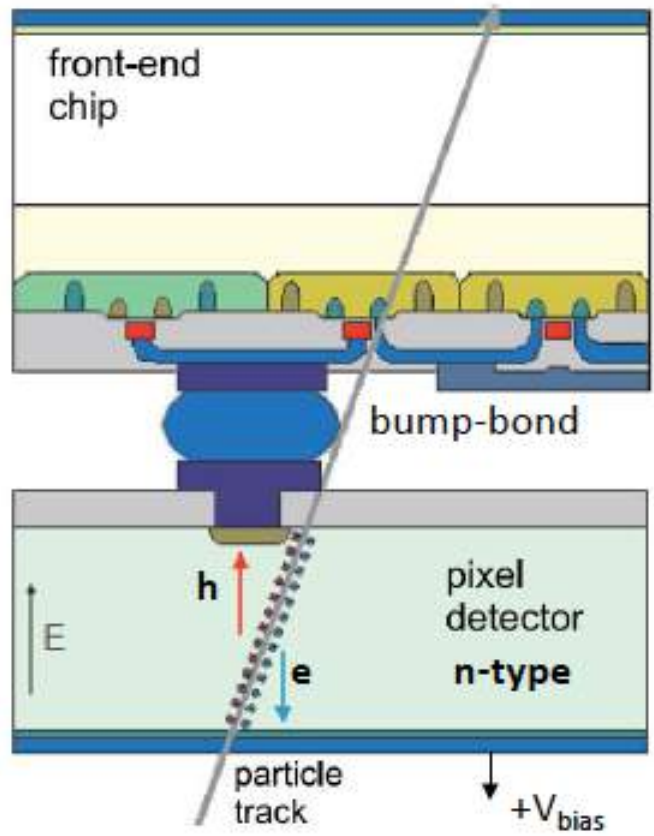
1. time schedule
2. Low cost
3. Low power consumption
4. Low material

# Pixel developments for ATLAS at HL-LHC. From Hybrid detectors to depleted Monolithic detectors

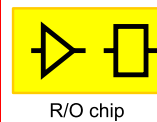


## Hybrid pixels

- Sensor + front-end chip separated entities
- Signal collected by drift
- Mature technology (in use since LEP 1996)



© T. Hemperek, Bonn, DE

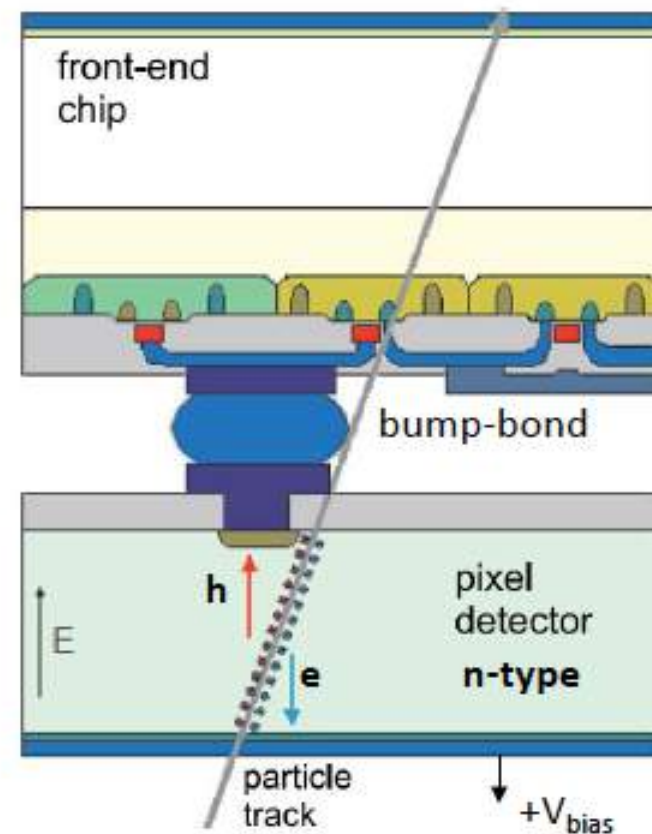


## Hybrid pixels

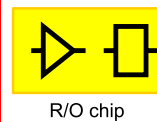
- Sensor + front-end chip separated entities
- Signal collected by drift
- Mature technology (in use since LEP 1996)

## Advantages

- Complex signal processing already in pixel cell possible
  - zero suppression, temporary storage of hits during L1 latency
- Radiation hard to  $> 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$
- High rate capability ( $\sim \text{MHz}/\text{mm}^2$ )



© T. Hemperek, Bonn, DE



## Hybrid pixels

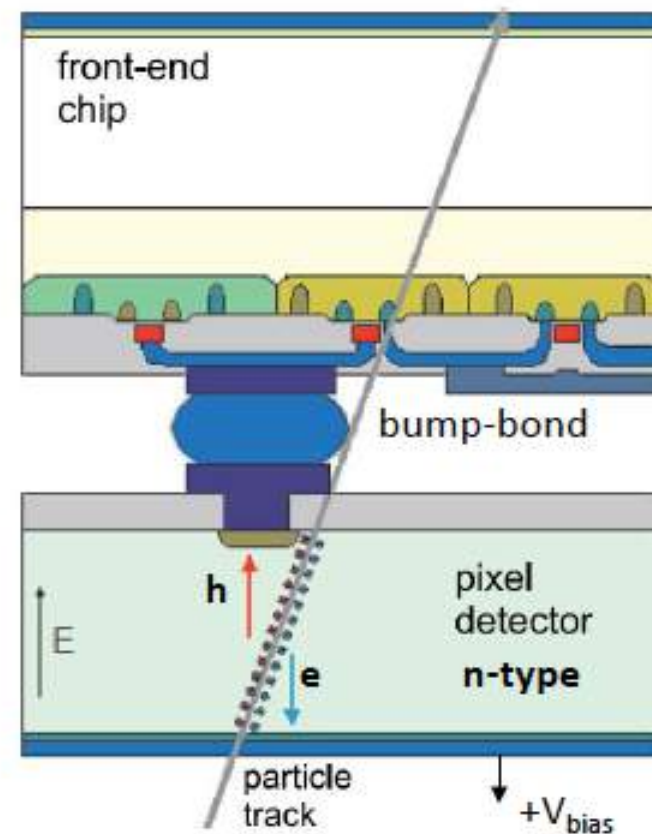
- Sensor + front-end chip separated entities
- Signal collected by drift
- Mature technology (in use since LEP 1996)

## Advantages

- Complex signal processing already in pixel cell possible
  - zero suppression, temporary storage of hits during L1 latency
- Radiation hard to  $> 10^{15} n_{eq}/cm^2$
- High rate capability ( $\sim MHz/mm^2$ )

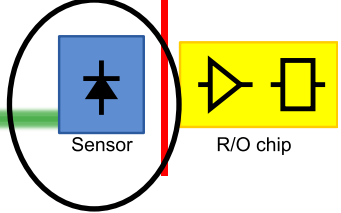
## Disadvantages

- Complex and laborious module production
  - Many production steps  $\rightarrow$  low production yield
  - Bump-bonding / flip-chipping  $\rightarrow$  limiting pixel size
  - Expensive
- Relatively large material budget  $\sim 3\% X_0$  per layer
  - sensor + chip + flex kapton + passive components
  - support, cooling, services



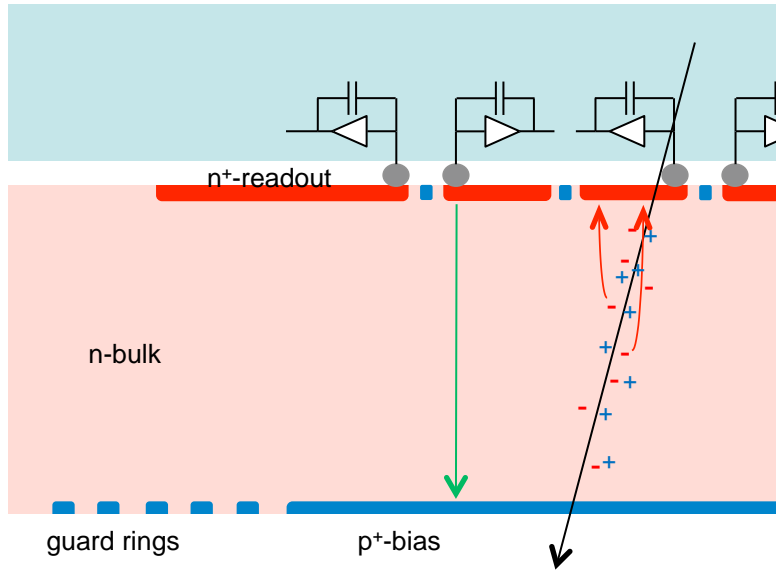
© T. Hemperek, Bonn, DE

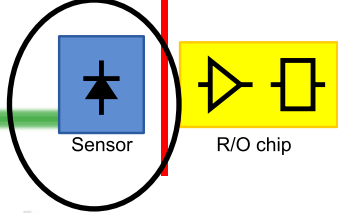




## Planar Pixel Sensor (PPS)

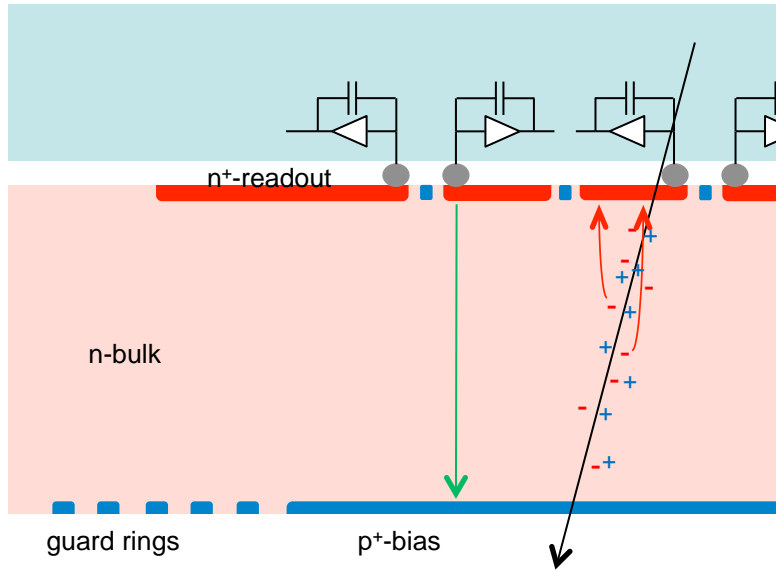
- Technology used in present Pixel Detector
- Collection distance = drift distance
- High production yield (%)
  - Large area sensors





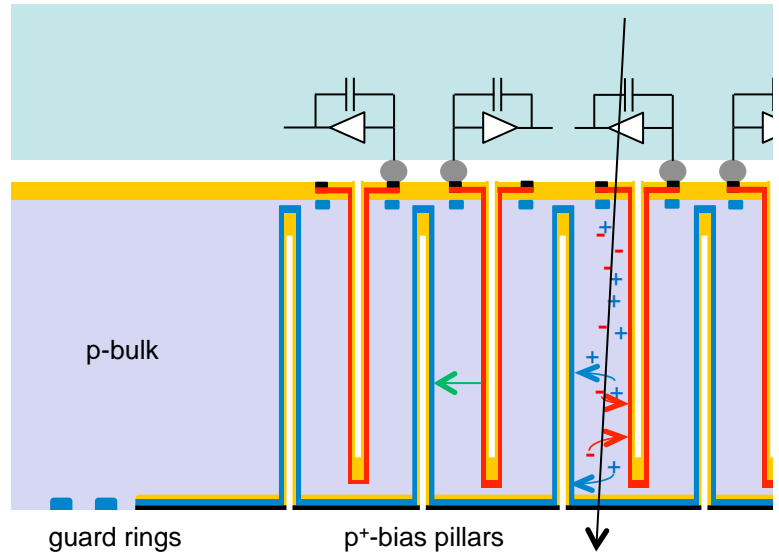
## Planar Pixel Sensor (PPS)

- Technology used in present Pixel Detector
- Collection distance = drift distance
- High production yield (%)
  - Large area sensors



## 3D Silicon Sensor (3D)

- Technology installed for the first time IBL
- Collection- and drift distance disconnected
- More difficult production, lower yield
  - Smaller area sensors

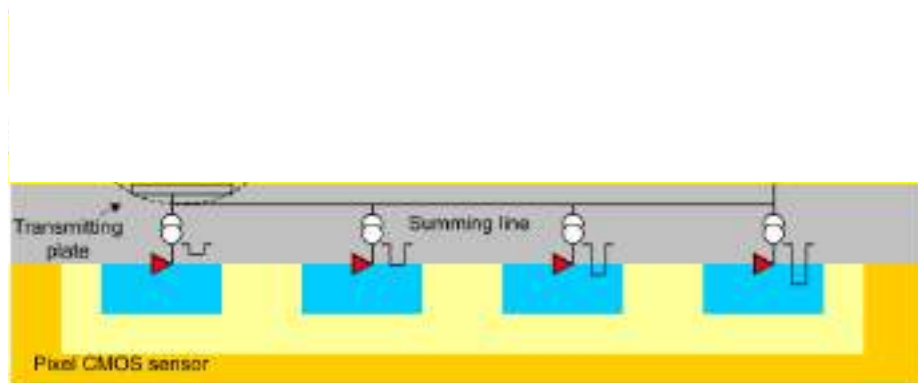


## CMOS-based pixels

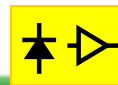
- Industrial process
  - higher production yield
  - cheaper sensors
- Collecting electrode inside → logic implementation in same silicon tile  
→ capacitive coupled connections, monolithic ...
  - smaller cost
  - smaller material budget
  - smaller pixel size
- There are two approaches

$$W = \sqrt{2 \epsilon \mu \rho V_b}$$

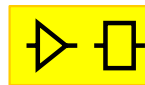
→ HV-CMOS  
→ HR-CMOS



- Both technologies are developed so far as hybrid approach



Diode +  
Preamp



R/O chip

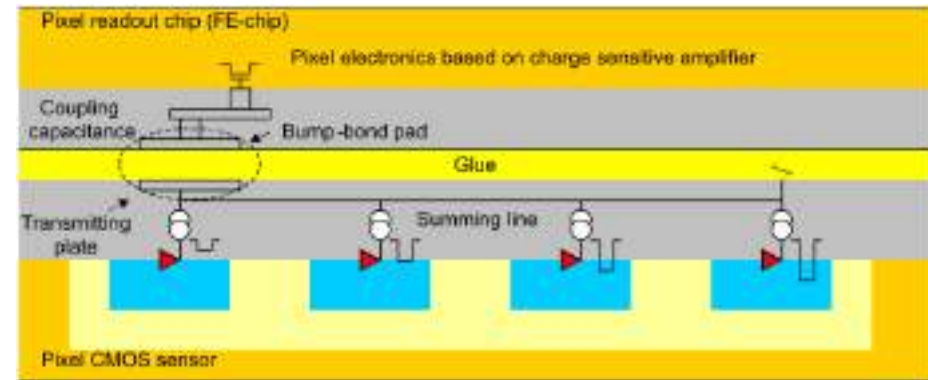
## CMOS-based pixels

- Industrial process
  - higher production yield
  - cheaper sensors
- Collecting electrode inside → logic implementation in same silicon tile  
→ capacitive coupled connections, monolithic ...
  - smaller cost
  - smaller material budget
  - smaller pixel size

- There are two approaches

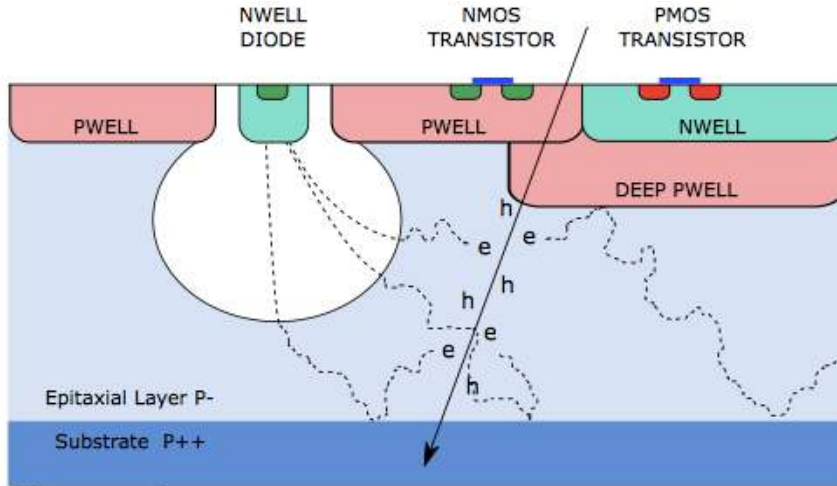
$$W = \sqrt{2 \epsilon \mu \rho V_b}$$

→ HV-CMOS  
→ HR-CMOS



- Both technologies are developed so far as hybrid approach

## MAPS epitaxial layer



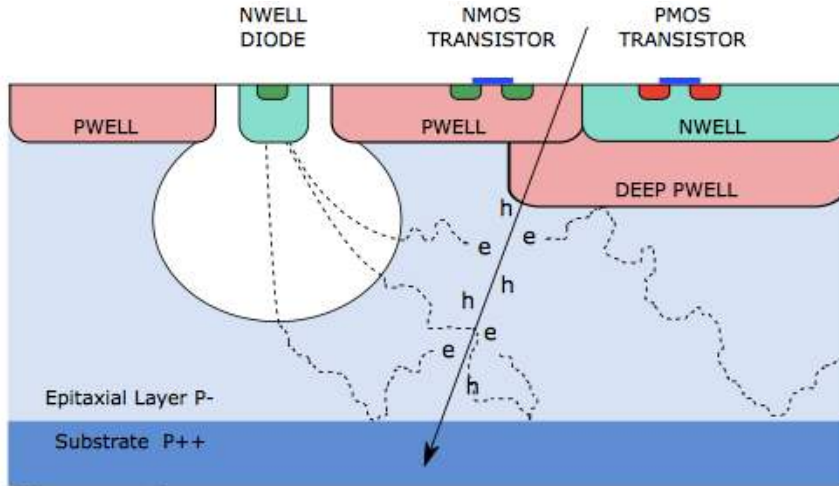
ALICE ITS (L. Mussa)

- Complex R/O electronics in sensor layer needed.
- High resistivity epitaxial layer
- Slow charge collection (diffusion)
- “low” radiation hardness
- STAR (2014), ALICE ITS (2018)



Diode + Amp + Digital

## MAPS epitaxial layer

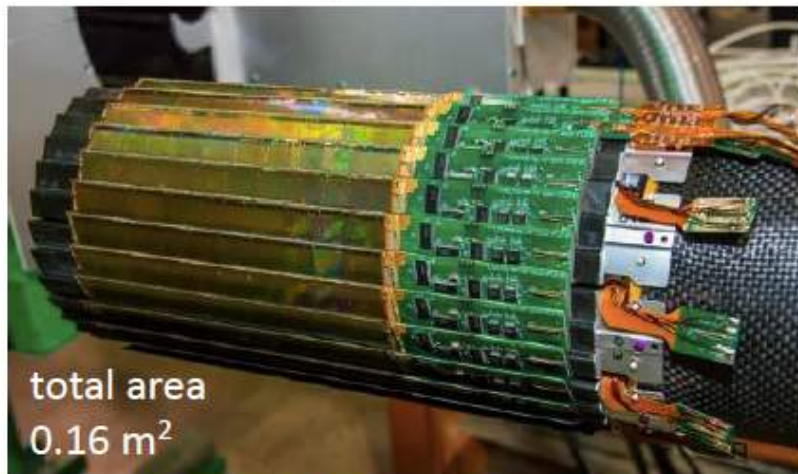


ALICE ITS (L. Mussa)

- Complex R/O electronics in sensor layer needed.
- High resistivity epitaxial layer
- Slow charge collection (diffusion)
- “low” radiation hardness
- STAR (2014), ALICE ITS (2018)

STAR / RHIC

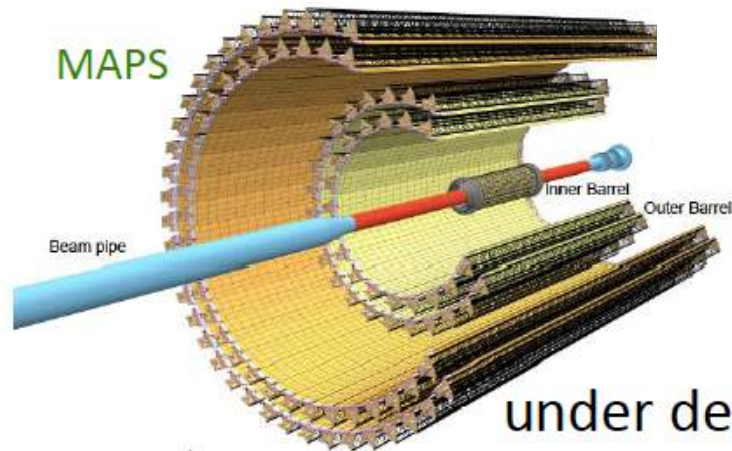
MAPS



total area  
0.16 m<sup>2</sup>

in operation since 2014

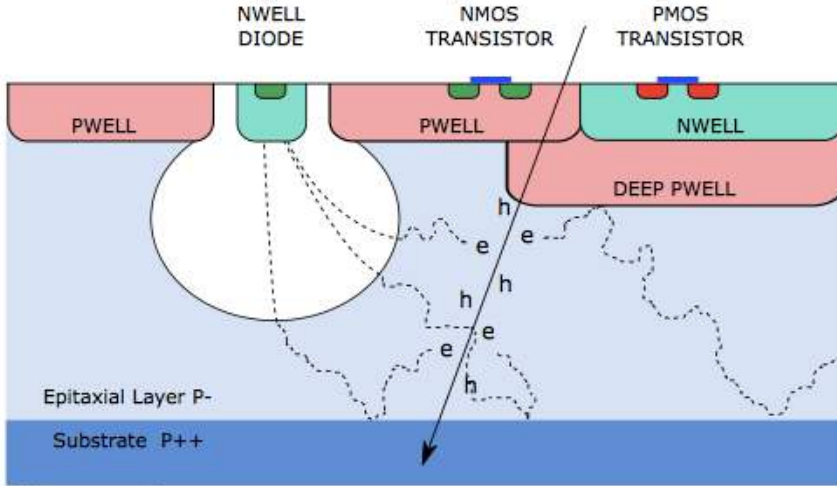
ALICE Upgrade



total area  
~10 m<sup>2</sup>

under development

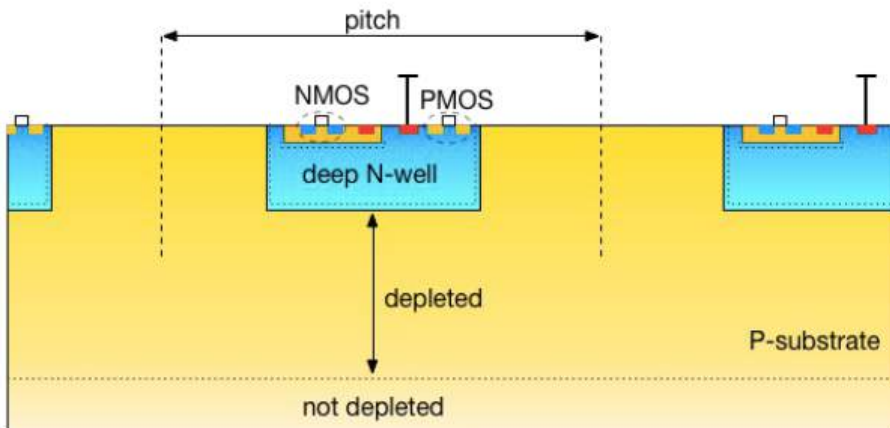
## MAPS epitaxial layer



ALICE ITS (L. Mussa)

- Complex R/O electronics in sensor layer needed.
- High resistivity epitaxial layer
- Slow charge collection (diffusion)
- “low” radiation hardness
- STAR (2014), ALICE ITS (2018)

## Depleted MAPS

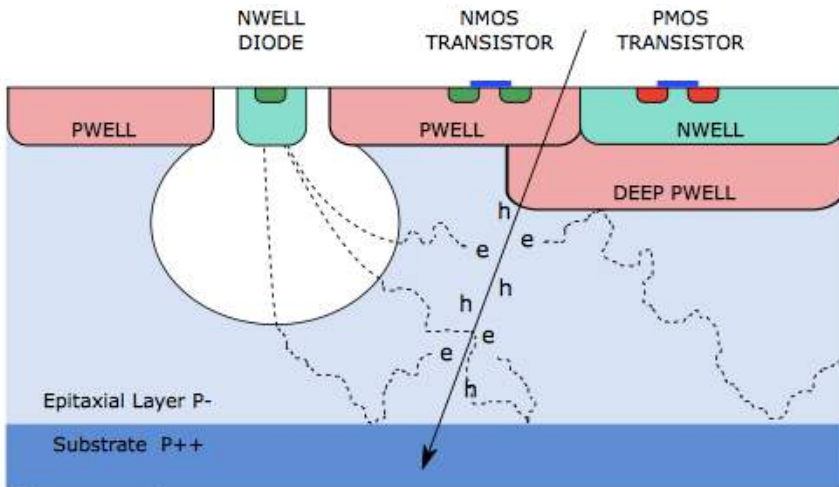


- Complex R/O electronics in sensor layer needed.
- High voltage/high resistivity process
- Fast charge collection (drift)
- [BELLE II DEPFET]



Diode + Amp + Digital

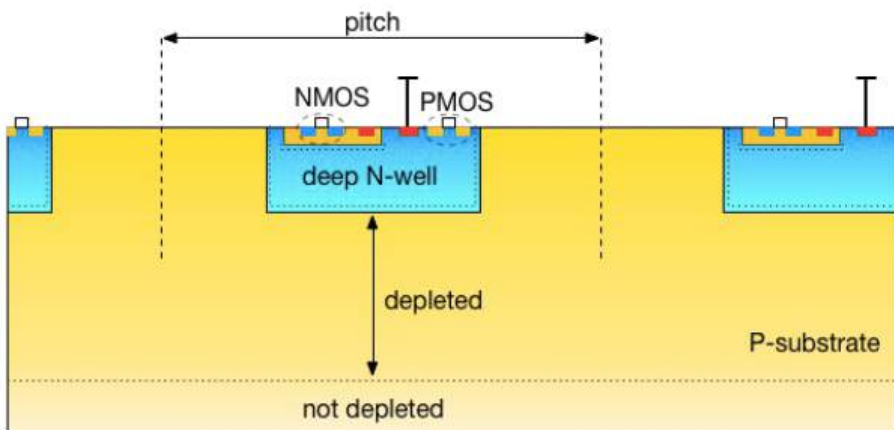
## MAPS epitaxial layer



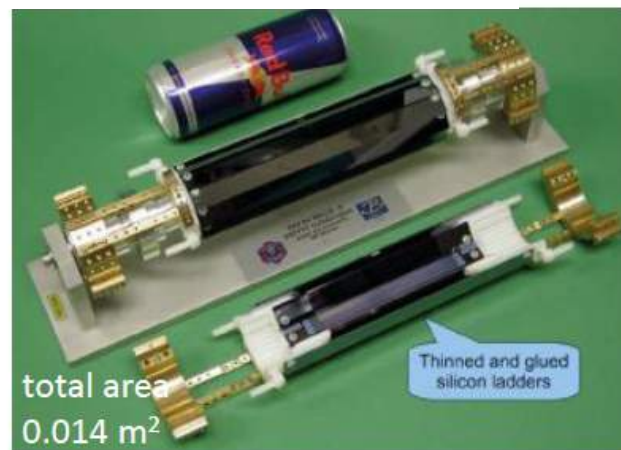
ALICE ITS (L. Mussa)

- Complex R/O electronics in sensor layer needed.
- High resistivity epitaxial layer
- Slow charge collection (diffusion)
- “low” radiation hardness
- STAR (2014), ALICE ITS (2018)

## Depleted MAPS



## Belle II (SuperKEK) DEPFET



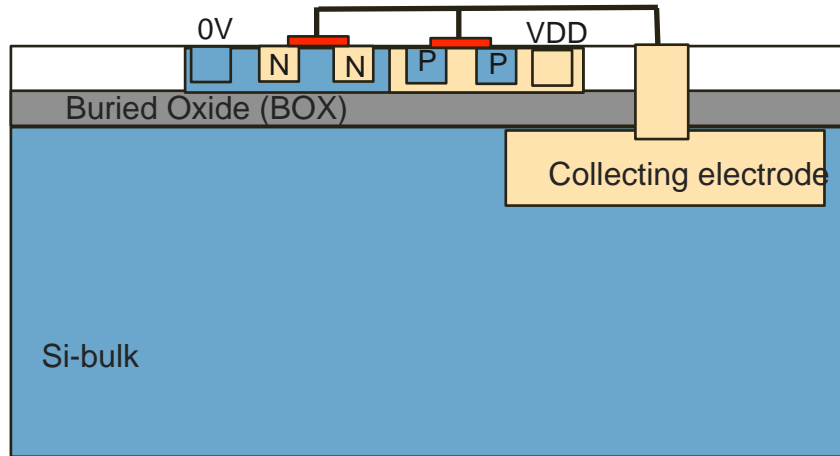
in production for 2017



## Depleted MAPS Silicon-On-Insulator

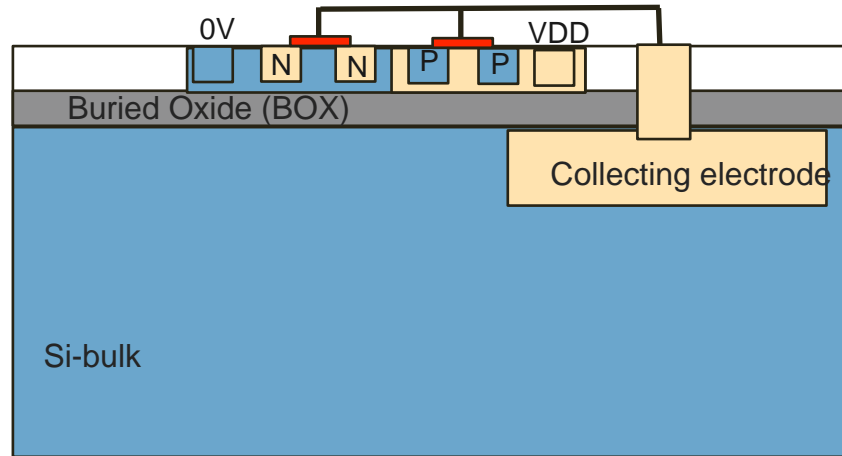


Diode + Amp + Digital



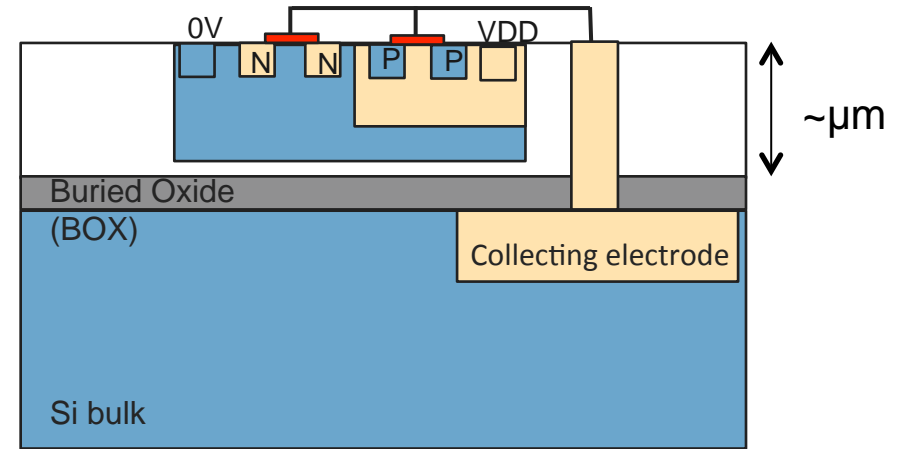
- Silicon-On-Insulator to separate logic from sensor diode. Several advantages:
  - Decoupling of electronics and sensor silicon resistivity
  - No competing N<sup>+</sup>WELL
  - Free choice of fill factor
  - Lower cross-talk
- Charge collection by drift

## Depleted MAPS Silicon-On-Insulator



### Standard

- Distance transistors-BOX  $\sim$ nm
- Ultra-thin transistor body  $\sim$ O(40 nm) FD
- Radiation hardness very challenging
- OKI/LAPIS



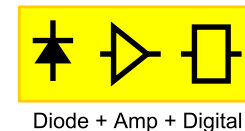
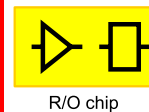
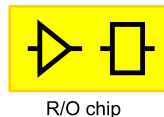
### Thick film

- Distance transistors-BOX  $\sim$  $\mu$ m
- Thick transistor body PD
- Multiple “wells” structures

*my thesis*

# Summary of pixel developments features

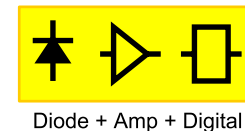
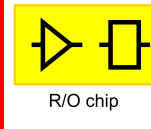
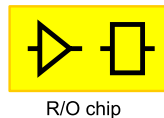
	Hybrid	CMOS pixels	Monolithic CMOS
Examples	3D, Planar (ATLAS, CMS, LHCvelo, Timepix3)	HV-CMOS HR-CMOS	MAPS (STAR, ALICE ITS) DMAPS SOI
Technology	Industry standard for readout; <b>special high-<math>\Omega</math> sensors</b>	R/O and sensors integrated, <b>close to industrial process</b>	R/O and sensor in <b>same piece of silicon</b> ; Industrial process
Interconnection	<b>Bump-bonding required</b>	<b>Connectivity facilitated</b> (CCPD) (or monolithic approach)	<b>No needed</b>
Granularity	<b>50 <math>\mu\text{m}</math> x 50 <math>\mu\text{m}</math></b>	<b>Down to few-micron sizes</b>	<b>Down to few-micron sizes</b>
Timing	<b>Fast</b>	<b>Coarse</b> but improving	<b>Coarse</b> but improving
Radiation hardness	<b>Feasible</b>	<b>To be proven</b>	<b>To be proven</b>



# Summary of pixel developments features

	Hybrid	CMOS pixels	Monolithic CMOS
Examples	3D, Planar (ATLAS, CMS, LHCvelo, Timenip)	HV-CMOS HR-CMOS	MAPS (STAR, ALICE ITS) DMAPS SOI
Technology	Industry standard for readout high resolution	R/O and sensors integrated, close to industrial process	R/O and sensor in same piece of silicon; Industrial process
Interconnectivity	High resolution High resolution	Connectivity facilitated (CCPD) (or monolithic approach)	No needed
Granularity	50 $\mu\text{m}$ x 50 $\mu\text{m}$	Down to few-micron sizes	Down to few-micron sizes
Timing	Fast	Coarse but improving	Coarse but improving
Radiation hardness	Feasible	To be proven	To be proven

inner pixel layers  
ATLAS ITk

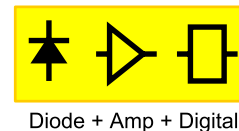
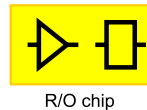
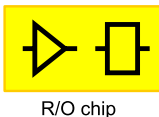


# Summary of pixel developments features

	Hybrid	CMOS pixels	Monolithic CMOS
Examples	3D, Planar (ATLAS, CMS, LHCVELO, Timepix)	HV-CMOS HR-CMOS	MAPS (STAR, ALICE ITS) DMAPS SOI
Technology	Industry standard for readout	R/O and sensors integrated, close to industrial processes	R/O and sensors in same process
Interconnectivity	High density routing	Connectivity facilitated by monolithic	High density routing
Granularity	50 $\mu\text{m}$ x 50 $\mu\text{m}$	Down to few-micron sizes	Down to few-micron sizes
Timing	Fast	Coarse but improving	Coarse but improving
Radiation hardness	Feasible	To be proven	To be proven

inner pixel layers  
ATLAS ITk

under investigation for  
outer pixel layers  
ATLAS ITk



# Visit CERN... Welcome!

Globe

Exhibitions

CERN Tours

Events

CERN shop

Contacts



# Careers at CERN

Work at CERN

Join us

Apply now

Tips for candidates

News

Media Corner

Professionals

Graduates

Students

Associates

**A great way to start your career!**

Job Search

Career

Level

Job

Category

Additional

text My Pro

Search  
Check

Thank for your attention



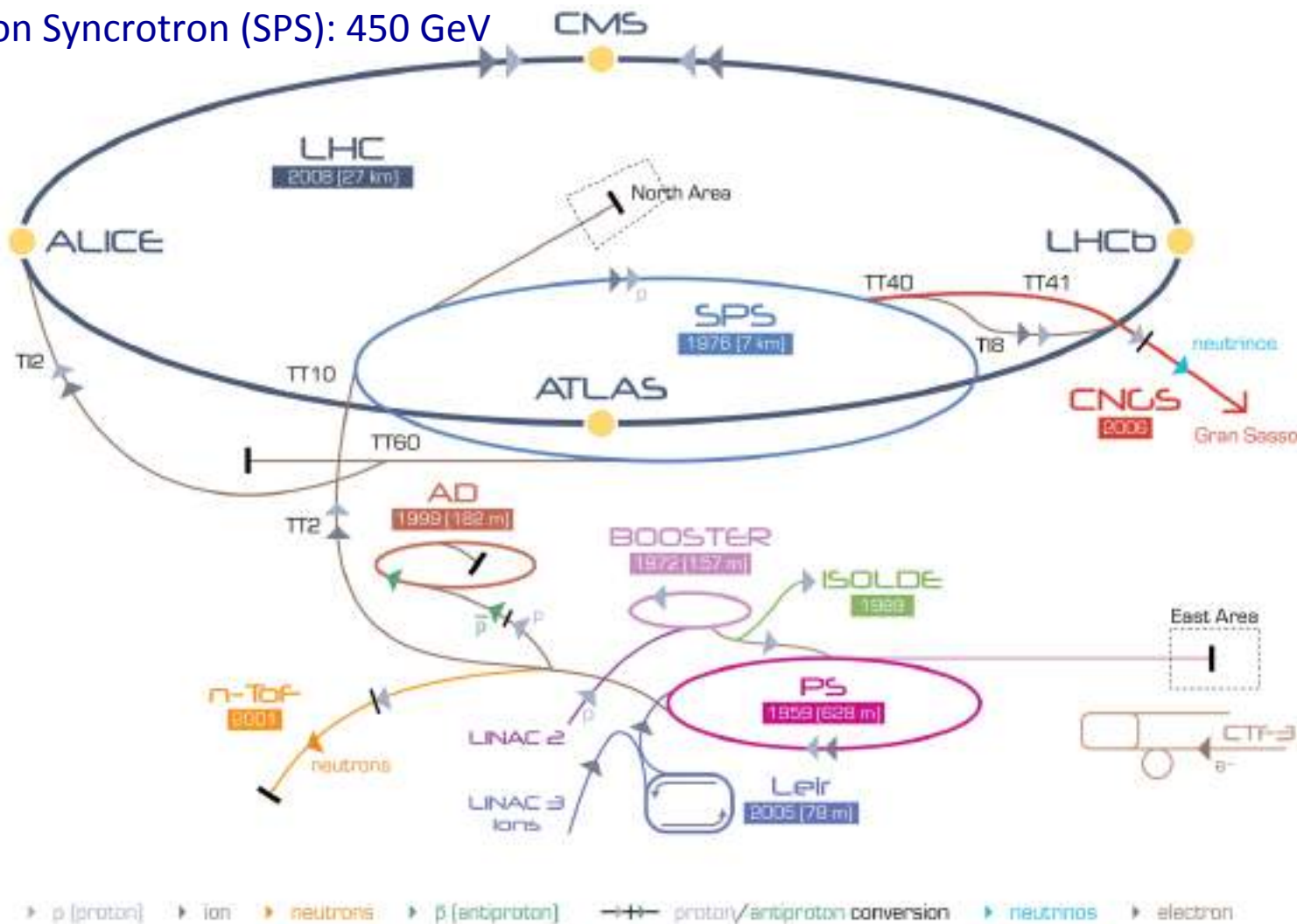
# Spare slides

LINAC 2: 50 MeV

Proton Synchrotron Booster (PSB): 1.4 GeV

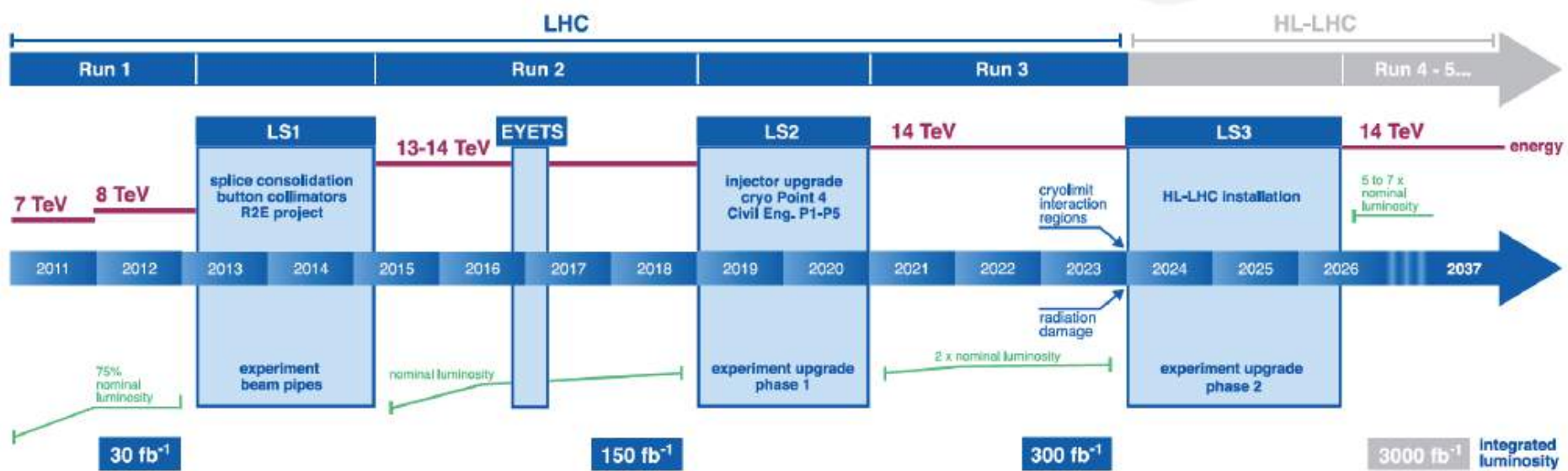
Proton Synchrotron (PS): 25 GeV

Super Proton Synchrotron (SPS): 450 GeV



LHC Large Hadron Collider SPS Super Proton Synchrotron PS Proton Synchrotron

AD Antiproton Decelerator CTF-3 Clic Test Facility CNCS CERN Neutrinos to Gran Sasso ISOLDE Isotope Separator OnLine DEvice  
LEIR Low Energy Ion Ring LINAC LINEar ACcelerator n-ToF Neutrons Time Of Flight



# Particle colliders requirements

[Slide by N. Wermes, Elba 2015]

	BX time	Particle Rate	NIEL Fluence	Ion. Dose
	ns	kHz/mm <sup>2</sup>	$n_{eq}/\text{cm}^2$ per lifetime*	Mrad per lifetime*
LHC ( $10^{34} \text{ cm}^{-2}\text{s}^{-1}$ )	25	1000	$2 \times 10^{15}$	79
HL-LHC ( $10^{35} \text{ cm}^{-2}\text{s}^{-1}$ )	25	10000	$2 \times 10^{16}$	> 500
LHC Heavy Ions ( $6 \times 10^{27} \text{ cm}^{-2} \text{ s}^{-1}$ )	20.000	10	$> 10^{13}$	0.7
RHIC ( $8 \times 10^{27} \text{ cm}^{-2}\text{s}^{-1}$ )	110	3.8	few $10^{12}$	0.2
SuperKEKB ( $10^{35} \text{ cm}^{-2}\text{s}^{-1}$ )	2	400	$\sim 3 \times 10^{12}$	10
ILC ( $10^{34} \text{ cm}^{-2}\text{s}^{-1}$ )	350	250	$10^{12}$	0.4

Monolithic Pixels

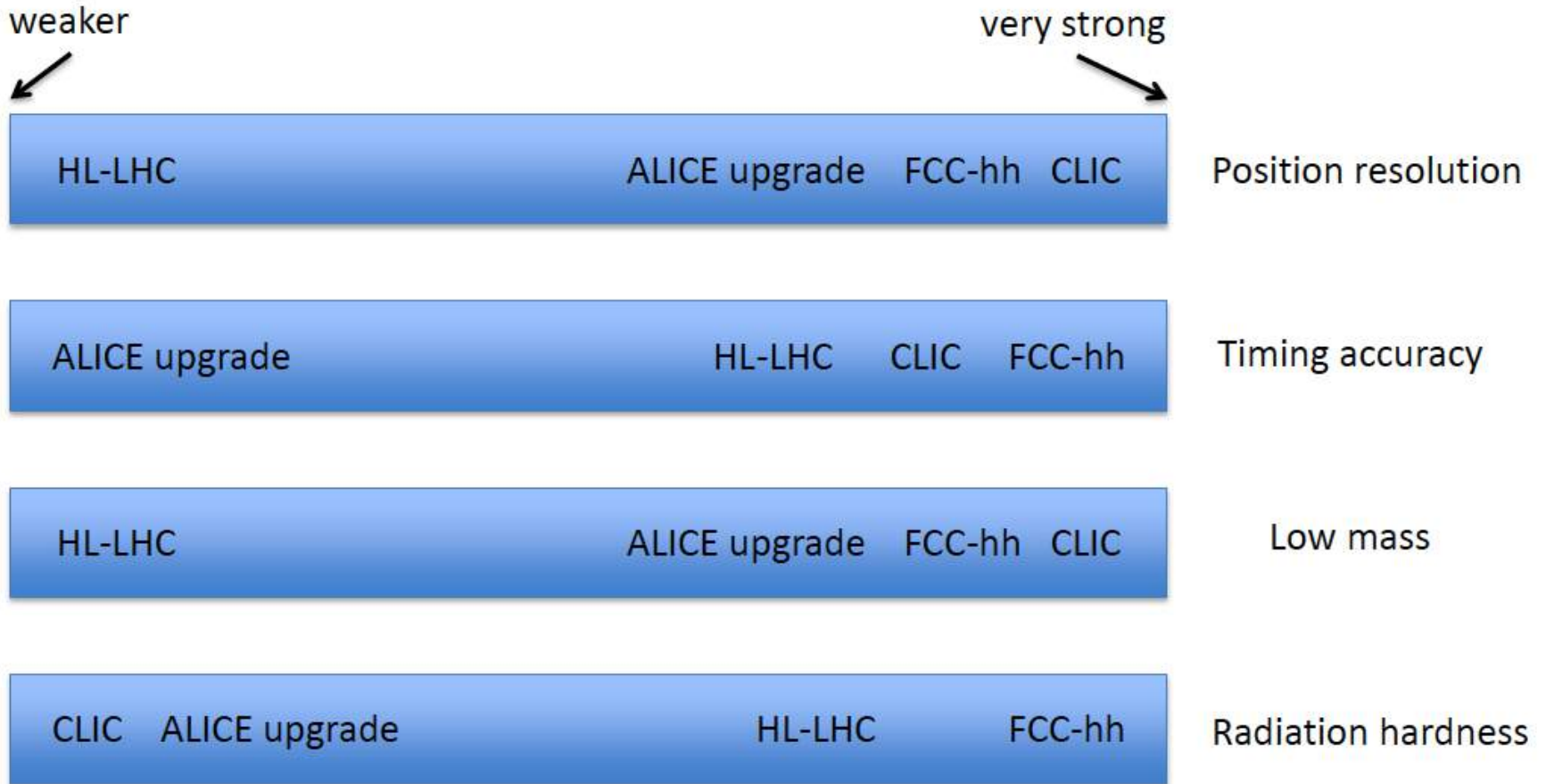
lower rates  
 lower radiation  
 smaller pixels  
 less material  
 better resolution

DEPFET: Belle II  
 MAPS: STAR@RHIC  
 and future  
 ALICE ITS

assumed lifetimes:  
 LHC, HL-LHC: 7 years  
 ILC: 10 years  
 others: 5 years



# comparison of requirements



*The 4 listed projects have many individual requirements in common, though their combination is different*

# Introduction Particle's tracking detectors

- Layers of segmented silicon detectors
- The energy loss by the particle while traversing the detector → electrical signal
- The loss of energy by charged particles in matter → inelastic collisions

## Charged particles ( $m \gg m_e$ )

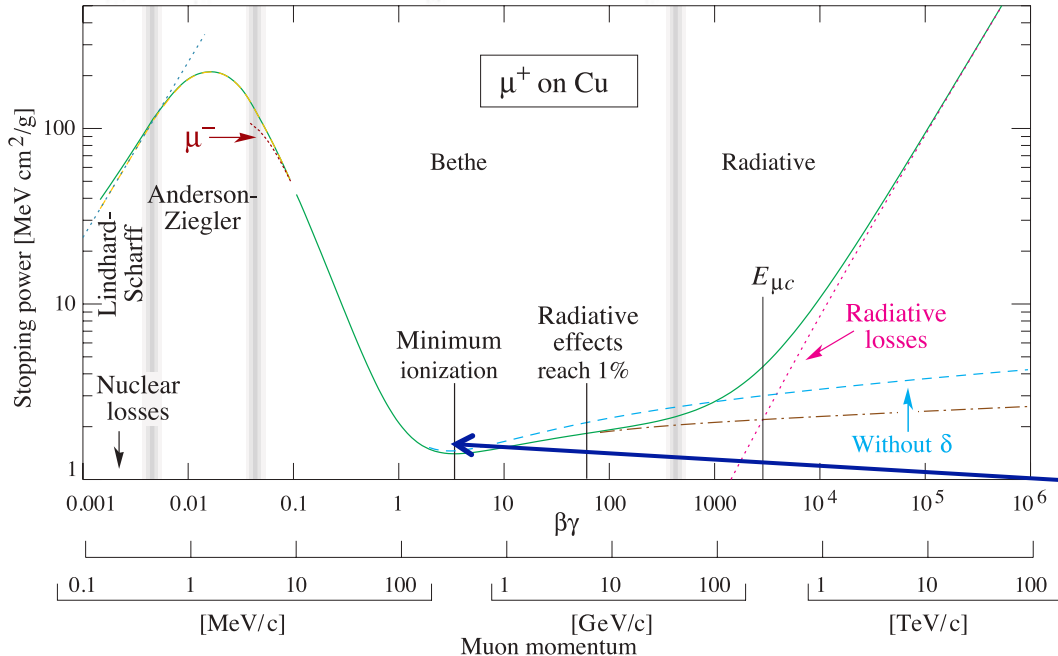
- Excitation and ionization of atoms
- Part of the energy is transferred to the atom
- Bethe-Bloch formula

$$-\frac{dE}{dx} = \frac{4\pi r_e^2 m_e c^2 N_A Z z^2}{A \beta^2} \cdot \left( \frac{1}{2} \ln \left( \frac{2m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} \right) - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right)$$

## Charged particles ( $m \sim m_e$ )

- Ionization of atoms + other
- At high energies → Bremsstrahlung dominates

$$-\left(\frac{dE}{dx}\right)_{rad} = \frac{E}{X_0}$$



MIP  
(Minimum Ionization Particle)

## Transverse momentum resolution

$$\frac{\sigma_{p_T}}{p_T} = \sqrt{\left(\frac{\sigma_{p_T}}{p_T}\right)_{point}^2 + \left(\frac{\sigma_{p_T}}{p_T}\right)_{MS}^2}$$

$$\frac{\sigma_{p_T}}{p_T}_{point} = p_T \cdot \frac{\sigma}{0.3BL^2} \cdot \sqrt{\frac{720N^3}{(N-1)(N+1)(N+2)(N+3)}}$$

$$\frac{\sigma_{p_T}}{p_T}_{MS} = \frac{1}{0.3B} \frac{0.0136}{\beta} \sqrt{\frac{C_N}{X_0L}}$$

## Vertex and Impact Parameter resolution

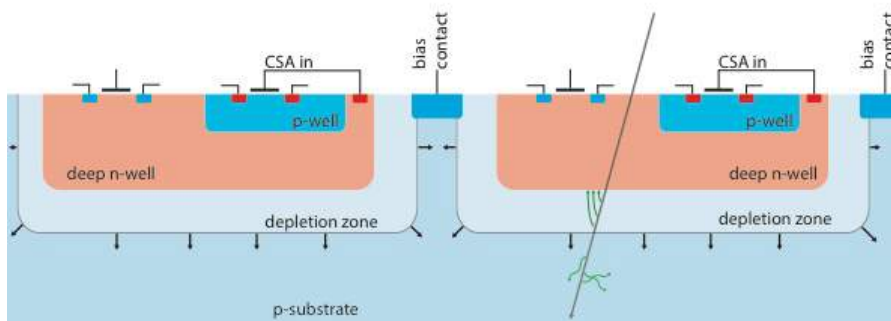
$$\sigma_{vtx}^2 \sim \frac{r_1^2 \sigma_1^2 + r_2^2 \sigma_2^2}{(r_2 - r_1)^2} + \frac{(2r_1 r_2 - r_0(r_1 + r_2))^2}{(r_2 - r_1)^2} \cdot \left(\frac{13.6 \text{ MeV}}{pv} \cdot \sqrt{\frac{d}{X_0}}\right)^2$$

$$\sigma_{d_0} = \sqrt{\frac{\sigma^2}{(N+1)} + \frac{\sigma^2}{(N+1)} \frac{12N}{(N+2)} \frac{z_c^2}{L^2}}; \quad z_c = (z_N - z_0)/2$$

- large detector coverage in  $\eta$
- a trade off between the material budget and the number of tracking layers
- location of the first layer as close as possible to the interaction point
- high magnetic field
- small detector and beam pipe thickness
- fine detector segmentation, specially in the layers close to the interaction point
- detector radiation hardness up to the expected fluences
- excellent detector efficiency which ensures a measurement point per detector layer
- high readout speed (25 ns in-time)

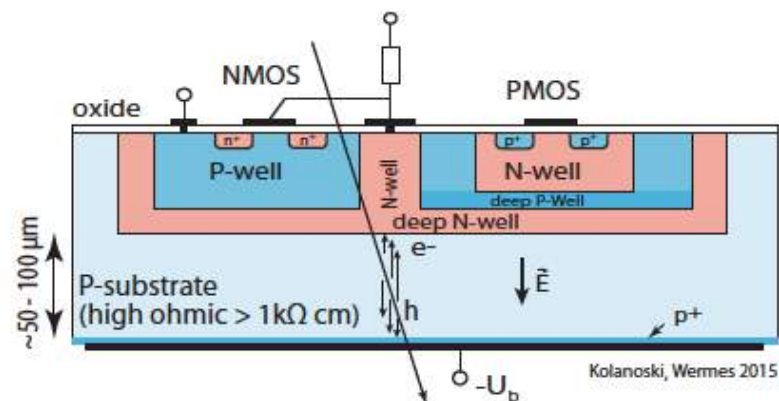


## HV-CMOS



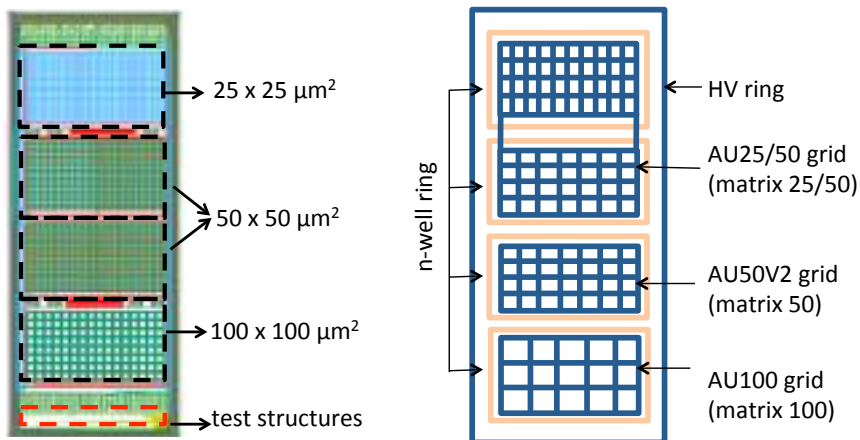
- HV technology (100V)
- Logic in-sensor
- Two approaches
  - Bump-bonded to dedicated R/O chip
  - Capacitive coupling via isolating glue
- Proven up to
  - 1GRad TID,  $10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$
  - 99% (96%) efficiency before (after) irr
  - depletion depth 10-20 $\mu\text{m}$  at 100V
  - signal rise-time 100ns
- A HV-CMOS prototype in 350nm produced in large scale (2x2cm)

## HR-CMOS



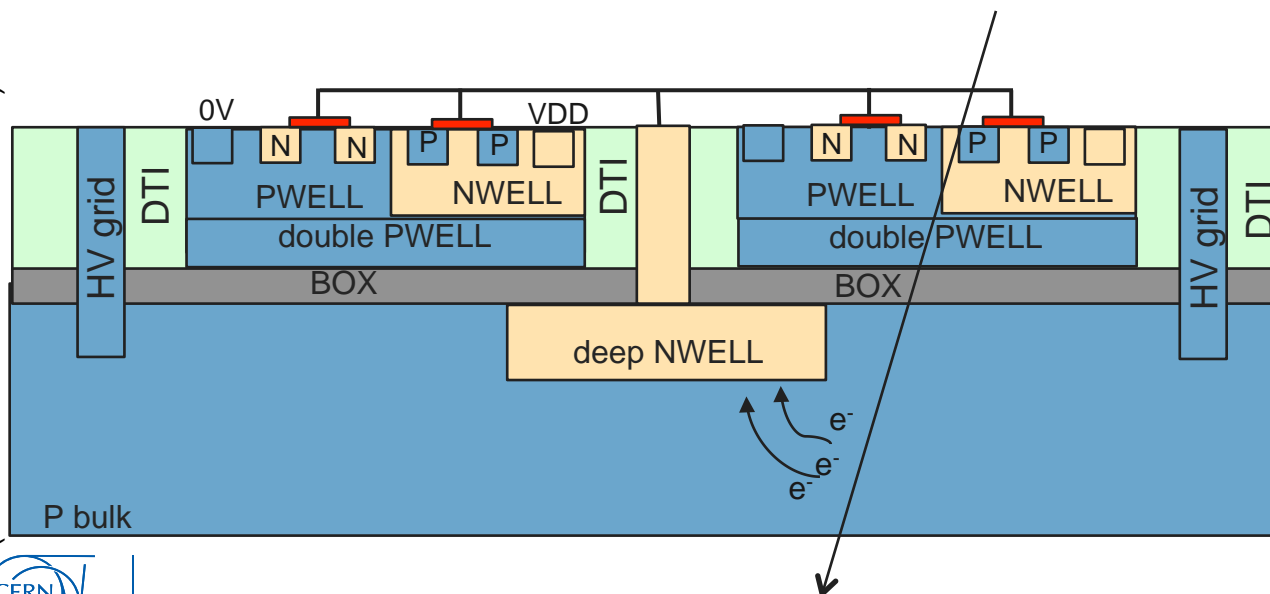
- High resistivity substrate (1-2 K $\Omega$  cm)
- Two variants are being investigated
  - different geometries
- Two approaches
  - Bump-bonded to dedicated R/O chip
  - Monolithic
- Proven up to
  - Depletion 60 $\mu\text{m}$  at 20V (6200e $^{-}$ )
  - Rise-time within 25ns (threshold dependency)
- A HR-CMOS prototype in 150nm selected  $\rightarrow$  production in large scale (2x2cm)

# XTB01 prototype



- 2 x 5 mm<sup>2</sup>
- 300  $\mu\text{m}$  thick
- 4 metal layers, wafer size: 8"
- Four matrices with different pixel sizes (25x25  $\mu\text{m}^2$ , 50x50  $\mu\text{m}^2$ , 100x100  $\mu\text{m}^2$ )
- Transistor test structures
- HV ring, grid rings, n-rings

(Pixel cross section. No to scale)



- thick film DMAPS SOI 0.18  $\mu\text{m}$
- BOX isolates sensor and electronics
- thick film, double PWELL
- no back-processing (HV applied from front side)
- MIP detection